Intel® Desktop Board D845GVFN

Technical Product Specification

August 2004

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The Intel® Desktop Board D845GVFN may contain design defects or errors known as errata that may cause the product to deviate from published specifications. Current characterized errata are documented in the Intel Desktop Board D845GVFN Specification Update.

Revision History

Revision	Revision History	Date
-001	First release of the Intel® Desktop Board D845GVFN Technical Product Specification.	August 2004

This product specification applies to only standard Intel® Desktop Board D845GVFN with BIOS identifier FN84510A.86A.

Changes to this specification will be published in the Intel Desktop Board D845GVFN Specification Update before being incorporated into a revision of this document.

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Preface

This Technical Product Specification (TPS) specifies the board layout, components, connectors, power and environmental requirements, and the BIOS for the Intel® Desktop Board D845GVFN. It describes the standard product and available manufacturing options.

Intended Audience

The TPS is intended to provide detailed, technical information about the Desktop Board D845GVFN and their components to the vendors, system integrators, and other engineers and technicians who need this level of information. It is specifically *not* intended for general audiences.

What This Document Contains

Chapter	Description
1	A description of the hardware used on the Desktop Board D845GVFN
2	A map of the resources of the desktop board
3	The features supported by the BIOS Setup program
4	A description of the BIOS error messages, beep codes, and POST codes

Typographical Conventions

This section contains information about the conventions used in this specification. Not all of these symbols and abbreviations appear in all specifications of this type.

Notes, Cautions, and Warnings

NOTE

Notes call attention to important information.

INTEGRATOR'S NOTES

Integrator's notes are used to call attention to information that may be useful to system integrators.

CAUTION

Cautions are included to help you avoid damaging hardware or losing data.

WARNING

Warnings indicate conditions, which if not observed, can cause personal injury.

Other Common Notation

#	Used after a signal name to identify an active-low signal (such as USBP0#)
(NxnX)	When used in the description of a component, N indicates component type, xn are the relative coordinates of its location on the Desktop Board D845GVFN, and X is the instance of the particular part at that general location. For example, J5J1 is a connector, located at 5J. It is the first connector in the 5J area.
GB	Gigabyte (1,073,741,824 bytes)
GB/sec	Gigabytes per second
KB	Kilobyte (1024 bytes)
Kbit	Kilobit (1024 bits)
kbits/sec	1000 bits per second
MB	Megabyte (1,048,576 bytes)
MB/sec	Megabytes per second
Mbit	Megabit (1,048,576 bits)
Mbit/sec	Megabits per second
xxh	An address or data value ending with a lowercase h indicates a hexadecimal value.
x.x V	Volts. Voltages are DC unless otherwise specified.
*	This symbol is used to indicate third-party brands and names that are the property of their respective owners.

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1 Product Description

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1.1 Overview

1.1.1 Feature Summary

Table 1 summarizes the major features of the Intel® Desktop Board D845GVFN.

Table 1. Feature Summary

Form Factor	microATX (9.20 inches by 8.20 inches [233.68 millimeters by 208.28 millimeters])
Processor	• Support for an Intel® Pentium® 4 processor in an mPGA478 socket with a 400/533 MHz system bus • Support for an Intel® Celeron® processor in an mPGA478 socket with a 400 MHz system bus
Memory	• Two 184-pin DDR SDRAM Dual Inline Memory Module (DIMM) sockets • Support for single-sided or double-sided DIMMs (DDR333/266/200) • Support for up to 2 GB system memory
Chipset	Intel® 845GV Chipset, consisting of: • Intel® 82845GV Graphics and Memory Controller Hub (GMCH) • Intel® 82801DB I/O Controller Hub (ICH4) • 3 Mbit Firmware Hub (FWH)
Video	Intel® Extreme Graphics controller
Audio	Audio subsystem for AC ‘97 processing using the Realtek ALC202A codec
I/O Control	SMSC LPC47M172 LPC Bus I/O controller or National Semiconductor PC87372 LPC Bus I/O controller
USB	Support for USB 2.0 devices
Peripheral Interfaces	• Up to four USB ports • One serial port • One parallel port • Two IDE interfaces with UDMA 33, ATA-66/100 support • One diskette drive interface • PS/2* keyboard and mouse ports • Three fan connectors
Expansion Capabilities	Three PCI bus add-in card connectors (SMBus routed to PCI bus connector 2)
BIOS	• Intel/AMI BIOS (resident in the 3 Mbit FWH) • Support for Advanced Configuration and Power Interface (ACPI), Plug and Play, and SMBIOS
Instantly Available PC Technology	• Support for PCI Local Bus Specification Revision 2.2 • Suspend to RAM support • Wake on PCI, RS-232, front panel, PS/2 devices, and USB ports

1.1.2 Manufacturing Options

Table 2 describes the manufacturing options on the Desktop Board D845GVFN. Not every manufacturing option is available in all marketing channels. Please contact your Intel representative to determine which manufacturing options are available to you.

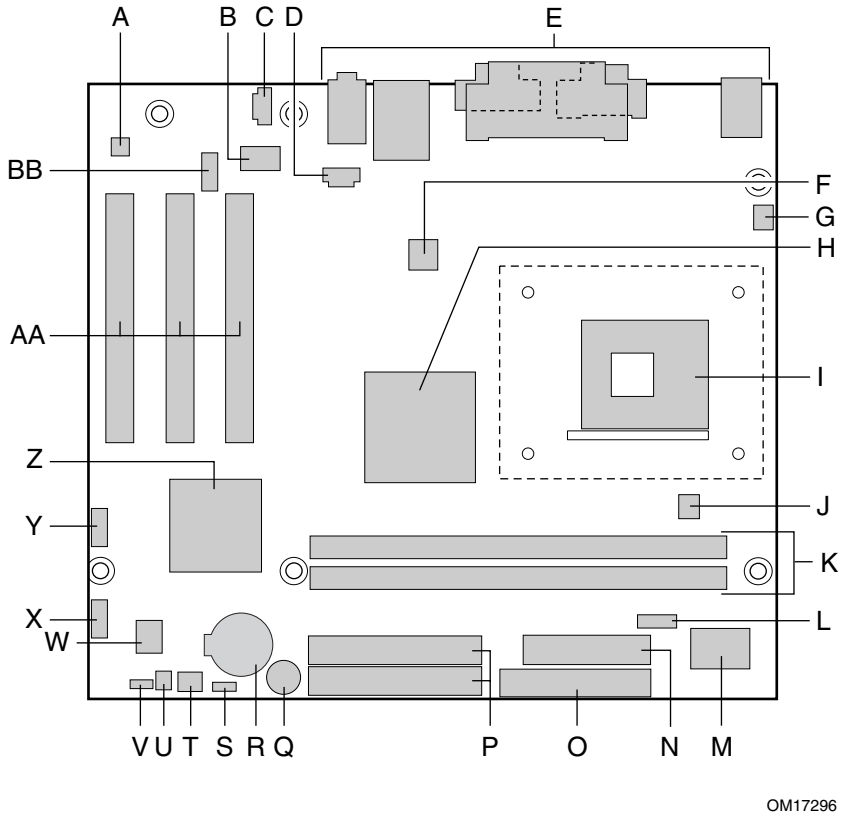
Table 2. Manufacturing Options

LAN	Intel® 82562ET 10/100 Mbit/sec Platform LAN Connect (PLC) device
Hardware Monitor Subsystem	• Hardware monitoring and fan control ASIC • Three fan sense inputs used to monitor fan activity • Chassis intrusion detection
Serial Port B	• Connector for a second serial port
ATAPI-style audio connectors	Two ATAPI-style audio connectors: • Auxiliary line input • ATAPI CD-DROM

For information about	Refer to
The board's compliance level with ACPI, Plug and Play, and SMBIOS	Section 1.5, page 15
Available configurations for the Desktop Board D845GVFN	Section 1.3, page 14

1.1.3 Board Layout

Figure 1 shows the location of the major components on the Desktop Board D845GVFN.



Item	Description	Item	Description
A	Audio codec	O	Diskette drive connector
B	Intel 82562ET 10/100 Mbit/sec (PLC) device (optional)	P	IDE connectors
C	Auxiliary line-in connector (optional)	Q	Speaker
D	ATAPI CD-ROM connector (optional)	R	Battery
E	Back panel connectors	S	Auxiliary front panel power LED connector
F	+12V power connector (ATX12V)	T	Front chassis fan connector
G	Rear chassis fan connector	U	Chassis intrusion connector (optional)
H	Intel 82845GV GMCH	V	BIOS Setup configuration jumper block
I	mPGA478 processor socket	W	3 Mbit Firmware Hub (FWH)
J	Processor fan connector	X	Front panel connector
K	DIMM sockets	Y	Front panel USB connector
L	Serial Port B connector (optional)	Z	Intel 82801DB I/O Controller Hub (ICH4)
M	I/O Controller	AA	PCI bus add-in card connectors
N	Power connector	BB	Front panel audio connector

Figure 1. Desktop Board D845GVFN Components

1.2 Block Diagram

Figure 2 is a block diagram of the major functional areas of the board.

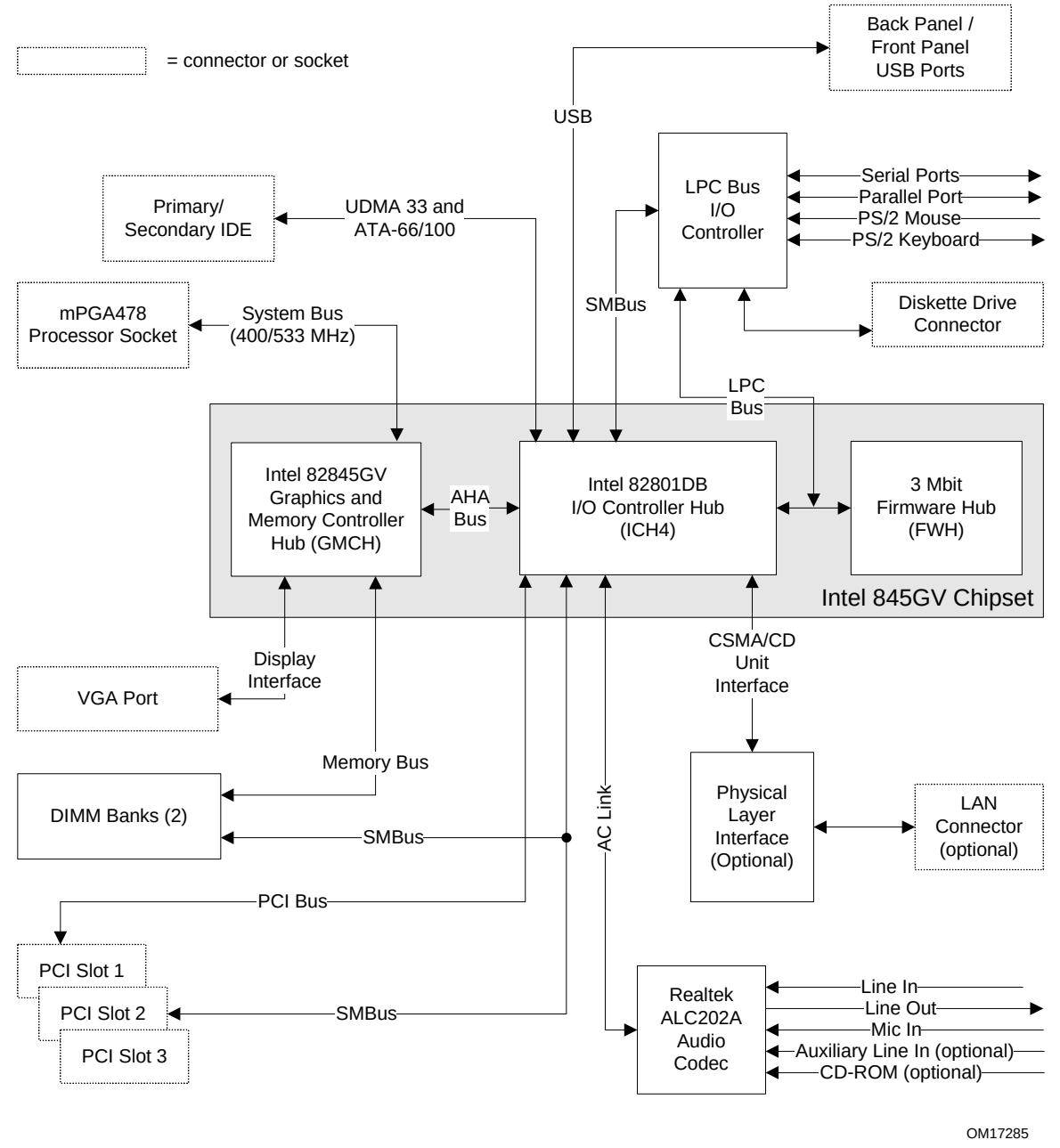


Figure 2. Block Diagram

1.3 Online Support

To find information about…	Visit this World Wide Web site:
Intel Desktop Board D845GVFN under "Desktop Board Products" or "Desktop Board Support"	http://www.intel.com/design/motherbd http://support.intel.com/support/motherboards/desktop
Available configurations for the Desktop Board D845GVFN	http://developer.intel.com/design/motherbd/fn/fn_available.htm
Processor data sheets	http://www.intel.com/design/litcentr
ICH4 addressing	http://developer.intel.com/design/chipsets/datashts
Custom splash screens	http://intel.com/design/motherbd/gen_indx.htm
Audio software and utilities	http://www.intel.com/design/motherbd
LAN software and drivers	http://www.intel.com/design/motherbd

1.4 Operating System Support

The Desktop Board D845GVFN supports drivers for all of the onboard hardware and subsystems under the following operating systems:

- Windows* XP
- Windows ME
- Windows 2000
- Microsoft Windows 98 SE

For information about	Refer to
Supported drivers	Section 1.3

NOTE

Third party vendors may offer other drivers.

1.5 Design Specifications

Table 3 lists the specifications applicable to the Desktop Board D845GVFN.

Table 3. Specifications

Reference Name	Specification Title	Version, Revision Date, and Ownership	The information is available from…
AC '97	*Audio Codec '97*	Revision 2.2, September 2000, Intel Corporation.	ftp://download.intel.com/labs/media/audio/download/ac97r22.pdf
ACPI	*Advanced Configuration and Power Interface Specification*	Version 1.0b, February 08, 1999, Intel Corporation, Microsoft Corporation, and Toshiba Corporation.	http://www.acpi.info/spec10b.htm
ASF	*Alert Standard Format (ASF) Specification*	Version 1.03, June 20, 2001, DMTF, Intel Corporation.	http://www.dmtf.org/standards/documents/ASF/DSP0114.pdf
ATA/ ATAPI-5	*Information Technology-AT Attachment with Packet Interface - 5* (ATA/ATAPI-5)	Revision 3, February 29, 2000, Contact: T13 Chair, Seagate Technology.	http://www.t13.org
ATX	*ATX Specification*	Version 2.03, December 1998, Intel Corporation.	http://www.formfactors.org/developer/specs/atx/atxspecs.htm
ATX12V	*ATX/ATX12V Power Supply Design Guide*	Version 1.2, August 2000, Intel Corporation.	http://www.formfactors.org/developer/specs/atx/atxspecs.htm
BIS	*Boot Integrity Services (BIS) Application Programming Interface (API)*	Version 1.0, August 4, 1999, Intel Corporation.	http://www.intel.com/labs/manage/wfm/wfmspecs.htm
DDR SDRAM	*Double Data Rate (DDR) SDRAM Specification*	Version 1.0, June 2000, JEDEC Solid State Technology Association.	http://www.jedec.org/
	Design Specification for a 184 Pin DDR Unbuffered DIMM	Revision 1.0, October 2001, JEDEC Solid State Technology Association.	http://www.jedec.org/
	Intel® JEDEC DDR 200/266 Unbuffered DIMM Specification Addendum	Revision 0.9, September 27, 2001, Intel Corporation.	http://developer.intel.com/technology/memory/index.htm

continued

Table 3. Specifications (continued)

Reference Name	Specification Title	Version, Revision Date and Ownership	The information is available from…
EHCI	*Enhanced Host Controller Interface Specification for Universal Serial Bus*	Revision 1.0, March 12, 2002, Intel Corporation.	http://developer.intel.com/technology/usb/download/ehci-r10.pdf
EPP	*IEEE Std 1284.1-1997* (Enhanced Parallel Port)	Version 1.7, 1997, Institute of Electrical and Electronic Engineers.	http://standards.ieee.org/reading/ieee/std_public/description/busarch/1284.1-1997_desc.html
El Torito	*Bootable CD-ROM Format Specification*	Version 1.0, January 25, 1995, Phoenix Technologies Limited and International Business Machines Corporation.	http://www.phoenix.com/resources/specs-cdrom.pdf
LPC	*Low Pin Count Interface Specification*	Revision 1.0, September 29, 1997, Intel Corporation.	http://www.intel.com/design/chipsets/industry/lpc.htm
MicroATX	*microATX Motherboard Interface Specification*	Version 1.0, December 1997, Intel Corporation.	http://www.formfactors.org/developer/specs/microatx/microatx.htm
PCI	*PCI Local Bus Specification*	Revision 2.2, December 18, 1998, PCI Special Interest Group.	http://www.pcisig.com/specifications
	PCI Bus Power Management Interface Specification	Revision 1.1, December 18, 1998, PCI Special Interest Group.	http://www.pcisig.com/specifications
Plug and Play	*Plug and Play BIOS Specification*	Version 1.0a, May 5, 1994, Compaq Computer Corporation, Phoenix Technologies Limited, and Intel Corporation.	http://www.microsoft.com/hwdev/tech/PnP/default.asp
PXE	*Preboot Execution Environment*	Version 2.1, September 20, 1999, Intel Corporation.	ftp://download.intel.com/labs/manage/wfm/download//pxespec.pdf
SFX	*SFX/SFX12V Power Supply Design Guide*	Version 2.0, May 2001, Intel Corporation.	http://www.formfactors.org/developer/specs/sfx/sfx12v.pdf

continued

Table 3. Specifications (continued)

Reference Name	Specification Title	Version, Revision Date and Ownership	The information is available from…
SMBIOS	*System Management BIOS*	Version 2.3.1, March 16, 1999, American Megatrends Incorporated, Award Software International Incorporated, Compaq Computer Corporation, Dell Computer Corporation, Hewlett-Packard Company, Intel Corporation, International Business Machines Corporation, Phoenix Technologies Limited, and SystemSoft Corporation.	http://www.dmtf.org/download/standards/DSP0119.pdf
TFX12V	*TFX12V Power Supply Design Guide*	Revision 1.01, May 2002 Intel Corporation	http://www.formfactors.org/developer/specs/tfx12v/tfx12v_psdg_101.pdf
UHCI	*Universal Host Controller Interface Design Guide*	Revision 1.1, March 1996, Intel Corporation.	http://developer.intel.com/design/USB/UHCI11D.htm
USB	*Universal Serial Bus Specification*	Revision 2.0, April 27, 2000, Compaq Computer Corporation, Hewlett-Packard Company, Lucent Technologies Inc., Intel Corporation, Microsoft Corporation, NEC Corporation, and Koninklijke Philips Electronics N.V.	http://www.usb.org/developers/docs.html
WfM	*Wired for Management Baseline*	Version 2.0, December 18, 1998, Intel Corporation.	http://www.intel.com/labs/manage/wfm/wfmspecs.htm

1.6 Processor

NOTE

Refer to Thermal Considerations (Section 2.12, page 61) for important information when using an Intel Pentium 4 processor operating above 2.80 GHz with this Intel desktop board.

The board is designed to support the following:

- Intel Pentium 4 processors in an mPGA478 processor socket with a 533/400 MHz system bus
- Intel Celeron processors in an mPGA478 processor socket with a 400 MHz system bus

See the Intel web site listed below for the most up-to-date list of supported processors.

For information about…	Refer to:
Supported processors for the D845GVFN board	http://www.intel.com/design/motherbd/fn/fn_proc.htm

CAUTION

Use only the processors listed on web site above. Use of unsupported processors can damage the board, the processor, and the power supply.

INTEGRATOR'S NOTES

- *Use only ATX12V-, SFX12V-, or TFX12V-compliant power supplies with the Desktop Board D845GVFN. ATX12V, SFX12V, and TFX12V power supplies have an additional power lead that provides required supplemental power for the processor. Always connect the 20-pin and 4-pin leads of ATX12V, SFX12V, and TFX12V power supplies to the corresponding connectors on the desktop board, otherwise the board will not boot.*
- *Do not use a standard ATX power supply. The board will not boot with a standard ATX power supply.*
- *Refer to Table 4 on page 19 for a list of supported system bus frequency and memory speed combinations.*

For information about	Refer to
Power supply connectors	Section 2.8.2.2, page 48

1.7 System Memory

The Desktop Board D845GVFN has two DIMM sockets and supports the following memory features:

- 2.5 V (only) 184-pin DDR SDRAM DIMMs with gold-plated contacts
- Unbuffered single-sided or double-sided DIMMs
- Maximum total system memory: 2 GB; minimum total system memory: 64 MB
- DDR333/266/200 MHz SDRAM DIMMs only
- Serial Presence Detect (SPD)
- Suspend to RAM

Table 4 lists the supported system bus frequency and memory speed combinations.

Table 4. Supported System Bus Frequency and Memory Speed Combinations

If the processor's system bus frequency is…	You can use this type of DIMM…
533 MHz	DDR333 or DDR266
400 MHz	DDR266 or DDR200

CAUTION

Do not use ECC DIMMs with this board. Using ECC DIMMs could damage the board.

INTEGRATOR'S NOTES

- *Registered DIMMs are not supported.*
- *Double-sided x16 DIMMs are not supported.*

NOTE

To be fully compliant with all applicable DDR SDRAM memory specifications, the board should be populated with DIMMs that support the Serial Presence Detect (SPD) data structure. This allows the BIOS to read the SPD data and program the chipset to accurately configure memory settings for optimum performance.

For information about	Refer to
Obtaining DDR SDRAM specifications	Section 1.5, page 15
Obtaining the PC Serial Presence Detect (SPD) Specification	Section 1.5, page 15

Table 5 lists the supported DDR DIMM configurations.

Table 5. Supported DDR DIMM Configurations

DIMM Capacity	Configuration (Note)	DDR SDRAM Density	DDR SDRAM Organization Front-side/Back-side	Number of DDR SDRAM Devices
64 MB	SS	64 Mbit	8 M x 8/empty	8
64 MB	SS	128 Mbit	8 M x 16/empty	4
128 MB	DS	64 Mbit	8 M x 8/8 M x 8	16
128 MB	SS	128 Mbit	16 M x 8/empty	8
128 MB	SS	256 Mbit	16 M x 16/empty	4
256 MB	DS	128 Mbit	16 M x 8/16 M x 8	16
256 MB	SS	256 Mbit	32 M x 8/empty	8
256 MB	SS	512 Mbit	32 M x 16/empty	4
512 MB	DS	256 Mbit	32 M x 8/32 M x 8	16
512 MB	SS	512 Mbit	64 M x 8/empty	8
1024 MB	DS	512 Mbit	64 M x 8/64 M x 8	16

Note: In this column, “DS” refers to double-sided memory modules (containing DDR SDRAM devices on both sides) and “SS” refers to single-sided memory modules (containing DDR SDRAM devices on only one side).

1.8 Intel® 845GV Chipset

The Intel 845GV chipset consists of the following devices:

- Intel 82845GV Graphics and Memory Controller Hub (GMCH) with Accelerated Hub Architecture (AHA) bus
- Intel 82801DB I/O Controller Hub (ICH4) with AHA bus
- Firmware Hub (FWH)

The GMCH is a centralized controller for the system bus, the memory bus, the AGP bus, and the Accelerated Hub Architecture interface. The ICH4 is a centralized controller for the board's I/O paths. The FWH provides the nonvolatile storage of the BIOS.

For information about	Refer to
The Intel 845GV chipset	http://developer.intel.com/
Resources used by the chipset	Chapter 2

1.8.1 Intel® Extreme Graphics Controller

The Intel Extreme Graphics controller features the following:

- Integrated graphics controller
  - 32 bpp (Bits Per Pixel) graphics engine
  - 266 MHz core frequency
  - 256-bit internal data path for 2-D and 3-D graphics
  - Motion video acceleration
- 3-D graphics visual and texturing enhancement
- Display
  - Integrated 24-bit 350 MHz RAMDAC
  - DDC2B compliant interface
- Video
  - Dual monitor synchronous display
  - Hardware motion compensation for software MPEG2 decode
- Dynamic Video Memory Technology (DVMT) support up to 64 MB

For information about	Refer to
DVMT	Section 1.8.1.1, page 25

Table 6 lists the Direct Draw supported modes.

Table 6. Direct Draw Supported Modes

Resolution	Color Palette	Refresh Frequency (Hz)	Notes
320 x 200	256 colors	70	Y
	64 K colors	70	3
	16 M colors	70	3
320 x 240	256 colors	70	Y
	64 K colors	70	3
	16 M colors	70	3
352 x 480	256 colors	70	Y
	64 K colors	70	3
	16 M colors	70	3
352 x 576	256 colors	70	Y
	64 K colors	70	3
	16 M colors	70	3
400 x 300	256 colors	70	Y
	64 K colors	70	3
	16 M colors	70	3
512 x 384	256 colors	70	Y
	64 K colors	70	3
	16 M colors	70	3
640 x 400	256 colors	70	Y
	64 K colors	70	3
	16 M colors	70	3

Notes: Y = Supported in driver without Direct3D* and OpenGL*
3 = Direct3D and OpenGL

Table 7 lists the video BIOS video modes supported by the graphics subsystem.

Table 7. Video BIOS Video Modes Supported for Analog CRTs

Resolution	Color Palette	Available Refresh Frequencies (Hz)	Notes
320 x 200	16 colors	70	T, G, B
	256 colors	70	G, B
320 x 350	16 colors	70	T, B
360 x 400	16 colors	70	T, B
640 x 200	16 colors	70	T, G, B
640 x 350	16 colors	70	T, G, B
640 x 480	16 colors	60	G, B
	256 colors	60, 75, 85	G, B, L
	64 K colors	60, 75, 85	G, B, L
	16 M colors	60, 75, 85	G, B, L
720 x 400	16 colors	70	T, B
800 x 600	256 colors	60, 75, 85	G, B, L
	64 K colors	60, 75, 85	G, B, L
	16 M colors	60, 75, 85	G, B, L
1024 x 768	256 colors	60, 75, 85	G, B, L
	64 K colors	60, 75, 85	G, B, L
	16 M colors	60, 75, 85	G, B, L
1056 x 350	16 colors	70	T, B
1056 x 400	16 colors	70	T, B
1056 x 480	16 colors	70	T, B
1280 x 1024	256 colors	60, 75, 85	G, B, L
	64 K colors	60, 75, 85	G, B, L
	16 M colors	60, 75, 85	G, B, L
1600 x 1200	256 colors	60, 75, 85	G, B, L
	64 K colors	60, 75, 85	G, B, L
	16 M colors	60, 75, 85	G, B, L
1920 x 1440	256 colors	60, 75	G, B, L
	64 K colors	60, 75	G, B, L

Notes: T = Text mode
G = Graphics mode
B = Banked addressing mode
L = Linear addressing mode

Table 8 lists the supported configuration modes of the graphics subsystem.

Table 8. Supported Configuration Modes

Resolution	Available Refresh Frequencies (Hz)	Supported bpp Configuration Mode (see Table 9 for more information)
640 x 480	60, 72, 75, 85, 100, 120	6
800 x 600	60, 72, 75, 85, 100, 120	6
1024 x 768	60, 70, 75, 85, 100	6
1024 x 768	120	5
1152 x 864	60, 75, 85	6
1152 x 864	100	5
1280 x 720	60, 75, 85	6
1280 x 720	100	5
1280 x 768	Reduced blanking	6
1280 x 960	60, 75	6
1280 x 960	85	5
1280 x 1024	60	6
1280 x 1024	75	5
1280 x 1024	85, 100	4
1280 x 1024	120	3
1400 x 1050	60	6
1600 x 900	60	6
1600 x 900	75, 85	4
1600 x 900	100	3
1600 x 1200	60	4
1600 x 1200	75, 85, 100	3
1856 x 1392	60, 75	3
1920 x 1080	60	4
1920 x 1080	75, 85	3
1920 x 1200	60	3
1920 x 1440	60, 75	3
2048 x 1536	60	3

Table 9 describes the bpp configuration mode values referenced in Table 8. In Table 9, assume that for each configuration mode number, the features of all lower numbers are also supported. For example, if the supported configuration mode is 4, then modes 1 through 3 are also supported. DVD consists of both the overlay engine as well as the MPEG decoding; both are necessary for DVD playback.

Table 9. Details of bpp Configuration Modes

Configuration Mode Number	Description
6	32 bpp (16 M colors) with DVD (Overlay + MPEG decode) On
5	16 bpp (64 K colors) with DVD On
4	32 bpp (16 M colors) with DVD Off
3	16 bpp (64 K colors) with DVD Off
2	8 bpp (256 colors) with DVD On
1	8 bpp (256 colors) with DVD off

For information about	Refer to
Obtaining graphics software and utilities	Section 1.3, page 14

1.8.1.1 Dynamic Video Memory Technology (DVMT)

DVMT enables enhanced graphics and memory performance through Direct AGP, and highly efficient memory utilization. DVMT ensures the most efficient use of available system memory (up to 64 MB) for maximum 2-D/3-D graphics performance.

DVMT uses a portion of system physical memory (as set in the BIOS Setup program) for compatibility with legacy applications. An example of this would be when using VGA graphics under DOS. Once loaded, the operating system and graphics drivers allocate the buffers needed for performing graphics functions.

NOTE

The use of DVMT requires operating system driver support.

For information about	Refer to
Obtaining the DVMT white paper	http://developer.intel.com/design/chipsets/845gv/

1.8.1.2 Zone Rendering Technology (ZRT)

The Intel Extreme Graphics Controller supports Zone Rendering Technology (ZRT). ZRT is a process by which the screen is divided into several zones. Each zone is completely cached and rendered on chip before being written to the frame buffer. The benefits of ZRT include the following:

- Increased memory efficiency via better localization of data
- Increased on-chip processing speed due to decreased wait time for data
- Increased effective pixel fill rates

- Increased headroom for larger resolution and color depth
- Reduced power as a result of decreased memory bandwidth
- Reduction in depth and color bandwidth associated with conventional rendering

For information about	Refer to
Obtaining the Zone Rendering white paper	http://developer.intel.com/design/chipsets/845gv/

1.8.2 USB

The board supports up to four USB 2.0 ports, fully supports UHCI and EHCI, and uses UHCI- and EHCI-compatible drivers. For more than four USB devices, an external hub can be connected to any of the ports.

The ICH4 provides the USB controller for all ports. The port arrangement is as follows:

- Two ports are implemented with stacked back panel connectors, adjacent to the audio connectors
- Two ports are routed to the front panel USB connector

NOTE

Computer systems that have an unshielded cable attached to a USB port may not meet FCC Class B requirements, even if no device is attached to the cable. Use shielded cable that meets the requirements for full-speed devices.

1.8.3 IDE Interfaces

The ICH4's IDE controller has two independent bus-mastering IDE interfaces that can be independently enabled. The IDE interfaces support the following modes:

- Programmed I/O (PIO): processor controls data transfer.
- 8237-style DMA: DMA offloads the processor, supporting transfer rates of up to 16 MB/sec.
- Ultra DMA: DMA protocol on IDE bus supporting host and target throttling and transfer rates of up to 33 MB/sec.
- ATA-66: DMA protocol on IDE bus supporting host and target throttling and transfer rates of up to 66 MB/sec. ATA-66 protocol is similar to Ultra DMA and is device driver compatible.
- ATA-100: DMA protocol on IDE bus allows host and target throttling. The ICH4's ATA-100 logic can achieve transfer rates up to 100 MB/sec.

INTEGRATOR'S NOTE

ATA-66 and ATA-100 are faster timings and require a specialized cable to reduce reflections, noise, and inductive coupling.

The IDE interfaces also support ATAPI devices (such as CD-ROM drives) and ATA devices.

The BIOS supports 48-bit Logical Block Addressing (LBA) and Extended Cylinder Head Sector (ECHS) translation modes. The drive reports the transfer rate and translation mode to the BIOS.

The desktop boards support Laser Servo (LS-120) diskette technology through the IDE interfaces. The BIOS supports booting from an LS-120 drive.

NOTE

The BIOS will always recognize an LS-120 drive as an ATAPI floppy drive. To ensure correct operation, do not configure the drive as a hard disk drive.

1.8.4 Real-Time Clock, CMOS SRAM, and Battery

A coin-cell battery (CR2032) powers the real-time clock and CMOS memory. When the computer is not plugged into a wall socket, the battery has an estimated life of three years. When the computer is plugged in, the standby current from the power supply extends the life of the battery. The clock is accurate to ± 13 minutes/year at 25 ºC with 3.3 VSB applied.

INTEGRATOR'S NOTE

If the battery and AC power fail, custom defaults, if previously saved, will be loaded into CMOS RAM at power-on.

1.9 I/O Controller

The SMSC LPC47M172 or National Semiconductor PC87372 I/O controller provides the following features:

- One serial port
- One parallel port with Extended Capabilities Port (ECP) and Enhanced Parallel Port (EPP) support
- Serial IRQ interface compatible with serialized IRQ support for PCI systems
- PS/2-style mouse and keyboard interfaces
- Interface for one 1.44 MB or 2.88 MB diskette drive
- Intelligent power management, including a programmable wake-up event interface
- PCI power management support

The BIOS Setup program provides configuration options for the I/O controller.

For information about	Refer to
SMSC LPC47M172 I/O controller	http://www.smsc.com
National Semiconductor PC87372	http://www.national.com

1.9.1 Serial Ports

The desktop board has two serial port connectors. Serial port A is located on the back panel. Serial port B (optional) is accessible using a connector on the component side of the desktop board. The serial ports support data transfers at speeds up to 115.2 kbits/sec with BIOS support.

For information about	Refer to
The location of the serial port A connector	Figure 4, page 46
The location of the optional serial port B connector	Figure 7, page 52

1.9.2 Parallel Port

The 25-pin D-Sub parallel port connector is located on the back panel. Use the BIOS Setup program to set the parallel port mode.

1.9.3 Diskette Drive Controller

The I/O controller supports one diskette drive. Use the BIOS Setup program to configure the diskette drive interface.

1.9.4 Keyboard and Mouse Interface

PS/2 keyboard and mouse connectors are located on the back panel.

INTEGRATOR'S NOTE

The keyboard is supported in the bottom PS/2 connector and the mouse is supported in the top PS/2 connector. Power to the computer should be turned off before a keyboard or mouse is connected or disconnected.

1.10 Audio Subsystem

The audio subsystem consists of the following devices:

- Intel 82801DB I/O Controller Hub (ICH4)
- Realtek ALC202A audio codec

The audio subsystem includes these features:

- Signal-to-noise ratio ≥ 90 dB
- Supports wake events (driver dependent)
- Mic in pre-amp that supports dynamic, condenser, and electret microphones

The audio subsystem supports the following audio interfaces:

- Optional ATAPI-style connectors:
  - Auxiliary line in
  - CD-ROM
- Front panel audio connector, including pins for:
  - Line out
  - Mic in
- Back panel audio connectors:
  - Line out
  - Line in
  - Mic in

1.10.1 Audio Connectors

1.10.1.1 Front Panel Audio Connector

A 2 x 5-pin connector provides mic in and line out signals for front panel audio connectors.

For information about	Refer to
The location of the connector	Figure 5, page 48
The signal names of the front panel audio connector	Table 21, page 49
Obtaining the *Front Panel I/O Connectivity Design Guide*	Section 1.5, page 15

NOTE

The front panel audio connector is alternately used as a jumper block for routing audio signals. Refer to Section 2.9.1 on page 56 for more information.

1.10.1.2 Auxiliary Line In Connector (Optional)

An optional 1 x 4-pin ATAPI-style connector connects the left and right channel signals of an internal audio device to the audio subsystem.

For information about	Refer to
The location of the auxiliary line in connector	Figure 5, page 48
The signal names of the auxiliary line in connector	Table 22, page 49

1.10.1.3 ATAPI CD-ROM Audio Connector (Optional)

An optional 1 x 4-pin ATAPI-style connector connects an internal ATAPI CD-ROM drive to the audio mixer.

For information about	Refer to
The location of the ATAPI CD-ROM connector	Figure 5, page 48
The signal names of the ATAPI CD-ROM connector	Table 23, page 49

1.10.2 Audio Subsystem Software

Audio software and drivers are available from Intel's World Wide Web site.

For information about	Refer to
Obtaining audio software and drivers	Section 1.3, page 14

1.11 LAN Subsystem (Optional)

The Network Interface Controller subsystem consists of the ICH4 (with integrated LAN Media Access Controller) and a physical layer interface device. Features of the LAN subsystem include:

- PCI Bus Master interface
- CSMA/CD Protocol Engine
- Serial CSMA/CD unit interface that supports the 82562ET (10/100 Mbit/sec Ethernet)
- PCI Power Management
  - — Supports ACPI technology
  - — Supports LAN wake capabilities

1.11.1 Intel® 82562ET Platform LAN Connect Device

The Intel 82562ET component provides an interface to the back panel RJ-45 connector with integrated LEDs.

The Intel 82562ET provides the following functions:

- Basic 10/100 Ethernet LAN connectivity
- Supports RJ-45 connector with status indicator LEDs on the back panel
- Full device driver compatibility
- ACPI support
- Programmable transit threshold
- Configuration EEPROM that contains the MAC address

1.11.2 RJ-45 LAN Connector with Integrated LEDs

Two LEDs are built into the RJ-45 LAN connector. Table 10 describes the LED states when the desktop board is powered up and the LAN subsystem is operating.

Table 10. LAN Connector LED States

LED Color	LED State	Condition
Green	Off	10 Mbit/sec data rate is selected.
	On	100 Mbit/sec data rate is selected.
Yellow	Off	LAN link is not established.
	On (steady state)	LAN link is established.
	On (brighter and pulsing)	The computer is communicating with another computer on the LAN.

1.11.3 LAN Subsystem Software

LAN software and drivers are available from Intel's World Wide Web site.

For information about	Refer to
Obtaining LAN software and drivers	Section 1.3, page 14

1.12 Hardware Management Subsystem (Optional)

The hardware management features enable the boards to be compatible with the Wired for Management (WfM) specification. The board has several hardware management features, including the following:

- Fan monitoring (through the I/O controller or the hardware monitoring and fan control ASIC)
- Thermal and voltage monitoring
- Chassis intrusion detection

For information about	Refer to
The WfM specification	Section 1.5, page 15

1.12.1 Hardware Monitoring and Fan Control ASIC

The features of the hardware monitoring and fan control ASIC include:

- Internal ambient temperature sensor
- Two remote thermal diode sensors for direct monitoring of processor temperature and ambient temperature sensing
- Power supply monitoring of five voltages (+5 V, +12 V, +3.3 VSB, +1.5 V, and +VCCP) to detect levels above or below acceptable values
- Thermally monitored closed-loop fan control, for all three fans, that can adjust the fan speed or switch the fans on or off as needed
- SMBus interface
- Fan monitoring for all three fan connectors

1.12.2 Fan Monitoring

Fan monitoring can be implemented using Intel® LANDesk* Client Manager or third-party software.

For information about	Refer to
The functions of the fan connectors	Section 1.13.2.2, page 36

1.12.3 Chassis Intrusion and Detection

The board supports a chassis security feature that detects if the chassis cover is removed. The security feature uses a mechanical switch on the chassis that attaches to the chassis intrusion connector. When the chassis cover is removed, the mechanical switch is in the closed position.

1.13 Power Management

Power management is implemented at several levels, including:

- Software support through Advanced Configuration and Power Interface (ACPI)
- Hardware support:
  - Power connector
  - Fan connectors
  - LAN wake capabilities
  - Instantly Available PC technology
  - Resume on Ring
  - Wake from USB
  - Wake from PS/2 devices
  - Power Management Event signal (PME#) wake-up support

1.13.1 ACPI

ACPI gives the operating system direct control over the power management and Plug and Play functions of a computer. The use of ACPI with this board requires an operating system that provides full ACPI support. ACPI features include:

- Plug and Play (including bus and device enumeration)
- Power management control of individual devices, add-in boards (some add-in boards may require an ACPI-aware driver), video displays, and hard disk drives
- Methods for achieving less than 15-watt system operation in the power-on/standby sleeping state
- A Soft-off feature that enables the operating system to power-off the computer
- Support for multiple wake-up events (see Table 13 on page 34)
- Support for a front panel power and sleep mode switch

Table 11 lists the system states based on how long the power switch is pressed, depending on how ACPI is configured with an ACPI-aware operating system.

Table 11. Effects of Pressing the Power Switch

If the system is in this state…	…and the power switch is pressed for	…the system enters this state
Off (ACPI G2/G5 – Soft off)	Less than four seconds	Power-on (ACPI G0 – working state)
On (ACPI G0 – working state)	Less than four seconds	Soft-off/Standby (ACPI G1 – sleeping state)
On (ACPI G0 – working state)	More than four seconds	Fail safe power-off (ACPI G2/G5 – Soft off)
Sleep (ACPI G1 – sleeping state)	Less than four seconds	Wake-up (ACPI G0 – working state)
Sleep (ACPI G1 – sleeping state)	More than four seconds	Power-off (ACPI G2/G5 – Soft off)

For information about	Refer to
The desktop boards' compliance level with ACPI	Section 1.5, page 15

1.13.1.1 System States and Power States

Under ACPI, the operating system directs all system and device power state transitions. The operating system puts devices in and out of low-power states based on user preferences and knowledge of how devices are being used by applications. Devices that are not being used can be turned off. The operating system uses information from applications and user settings to put the system as a whole into a low-power state.

Table 12 lists the power states supported by the Desktop Board D845GVFN along with the associated system power targets. See the ACPI specification for a complete description of the various system and power states.

Table 12. Power States and Targeted System Power

Global States	Sleeping States	Processor States	Device States	Targeted System Power (Note 1)
G0 – working state	S0 – working	C0 – working	D0 – working state.	Full power > 30 W
G1 – sleeping state	S1 – Processor stopped	C1 – stop grant	D1, D2, D3 – device specification specific.	5 W < power < 52.5 W
G1 – sleeping state	S3 – Suspend to RAM. Context saved to RAM.	No power	D3 – no power except for wake-up logic.	Power < 5 W (Note 2)
G1 – sleeping state	S4 – Suspend to disk. Context saved to disk.	No power	D3 – no power except for wake-up logic.	Power < 5 W (Note 2)
G2/S5	S5 – Soft off. Context not saved. Cold boot is required.	No power	D3 – no power except for wake-up logic.	Power < 5 W (Note 2)
G3 – mechanical off AC power is disconnected from the computer.	No power to the system.	No power	D3 – no power for wake-up logic, except when provided by battery or external source.	No power to the system. Service can be performed safely.

Notes:

1. Total system power is dependent on the system configuration, including add-in boards and peripherals powered by the system chassis' power supply.
2. Dependent on the standby power consumption of wake-up devices used in the system.

1.13.1.2 Wake-up Devices and Events

Table 13 lists the devices or specific events that can wake the computer from specific states.

Table 13. Wake-up Devices and Events

These devices/events can wake up the computer…	…from this state
LAN	S1, S3, S4, S5 (Note)
Modem (back panel Serial Port A)	S1, S3
PME# signal	S1, S3, S4, S5 (Note)
Power switch	S1, S3, S4, S5
PS/2 devices	S1, S3
RTC alarm	S1, S3, S4, S5
USB	S1, S3

Note: For LAN and PME# signal, S5 is disabled by default in the BIOS Setup program. Setting this option to Power On will enable a wake-up event from LAN in the S5 state.

NOTE

The use of these wake-up events from an ACPI state requires an operating system that provides full ACPI support. In addition, software, drivers, and peripherals must fully support ACPI wake events.

1.13.2 Hardware Support

CAUTION

Ensure that the power supply provides adequate +5 V standby current if LAN wake capabilities and Instantly Available PC technology features are used. Failure to do so can damage the power supply. The total amount of standby current required depends on the wake devices supported and manufacturing options.

The Desktop Board D845GVFN provides several power management hardware features, including:

- Power connector
- Fan connectors
- LAN wake capabilities
- Instantly Available PC technology
- Resume on Ring
- Wake from USB
- Wake from PS/2 keyboard
- PME# signal wake-up support

LAN wake capabilities and Instantly Available PC technology require power from the +5 V standby line. The sections discussing these features describe the incremental standby power requirements for each.

Resume on Ring enables telephony devices to access the computer when it is in a power-managed state. The method used depends on the type of telephony device (external or internal).

NOTE

The use of Resume on Ring and Wake from USB technologies from an ACPI state requires an operating system that provides full ACPI support.

1.13.2.1 Power Connector

ATX12V-, SFX12V-, and TFX12V-compliant power supplies can turn off the system power through system control. When an ACPI-enabled system receives the correct command, the power supply removes all non-standby voltages.

When resuming from an AC power failure, the computer returns to the power state it was in before power was interrupted (on or off). The computer's response can be set using the Last Power State feature in the BIOS Setup program's Boot menu.

For information about	Refer to
The location of the power connector	Figure 5, page 48
The signal names of the power connector	Table 27, page 50
The ATX, SFX, and TFX12V specifications	Section 1.5, page 15

1.13.2.2 Fan Connectors

Table 14 summarizes the function/operation of the fan connectors.

Table 14. Fan Connector Function/Operation

Connector	Description
Processor fan	• +12 V DC connection for a processor fan or active fan heatsink. • Fan is on in the S0 or S1 state. Fan is off when the system is off or in the S3, S4, or S5 state. • Option to wire the fan tachometer input to the I/O controller or the Hardware Monitoring and Fan Control ASIC.
Front chassis fan	• +12 V DC connection for a system or chassis fan. • Fan is on in the S0 or S1 state. Fan is off when the system is off or in the S3, S4, or S5 state. • Option to wire the fan tachometer input to the Hardware Monitoring and Fan Control ASIC.
Rear chassis fan	• +12 V DC connection for a system or chassis fan. • Fan is on in the S0 or S1 state. Fan is off when the system is off or in the S3, S4, or S5 state. • Option to wire the fan tachometer input to the I/O controller or the Hardware Monitoring and Fan Control ASIC.

1.13.2.3 LAN Wake Capabilities

⚠ CAUTION

For LAN wake capabilities, the +5 V standby line for the power supply must be capable of providing adequate +5 V standby current. Failure to provide adequate standby current when implementing LAN wake capabilities can damage the power supply.

LAN wake capabilities enable remote wake-up of the computer through a network. The LAN subsystem PCI bus network adapter monitors network traffic at the Media Independent Interface. Upon detecting a Magic Packet* frame, the LAN subsystem asserts a wake-up signal that powers up the computer. Depending on the LAN implementation, the board supports LAN wake capabilities with ACPI in the following ways:

- The PCI bus PME# signal for PCI 2.2 compliant LAN designs
- The onboard LAN subsystem

1.13.2.4 Instantly Available PC Technology

⚠ CAUTION

For Instantly Available PC technology, the +5 V standby line for the power supply must be capable of providing adequate +5 V standby current. Failure to provide adequate standby current when implementing Instantly Available PC technology can damage the power supply.

Instantly Available PC technology enables the board to enter the ACPI S3 (Suspend-to-RAM) sleep-state. While in the S3 sleep-state, the computer will appear to be off (the power supply is off, and the front panel LED is amber if dual colored, or off if single colored.) When signaled by a wake-up device or event, the system quickly returns to its last known wake state. Table 13 on page 34 lists the devices and events that can wake the computer from the S3 state.

The board supports the *PCI Bus Power Management Interface Specification*. For information on the version of this specification, see Section 1.5.

Add-in boards that also support this specification can participate in power management and can be used to wake the computer.

The use of Instantly Available PC technology requires operating system support and PCI 2.2 compliant add-in cards and drivers.

1.13.2.5 +5 V Standby Power Indicator LED

The +5 V standby power indicator LED shows that power is still present even when the computer appears to be off. Figure 3 shows the location of the standby power indicator LED.

⚠ CAUTION

If AC power has been switched off and the standby power indicator is still lit, disconnect the power cord before installing or removing any devices connected to the board. Failure to do so could damage the board and any attached devices.

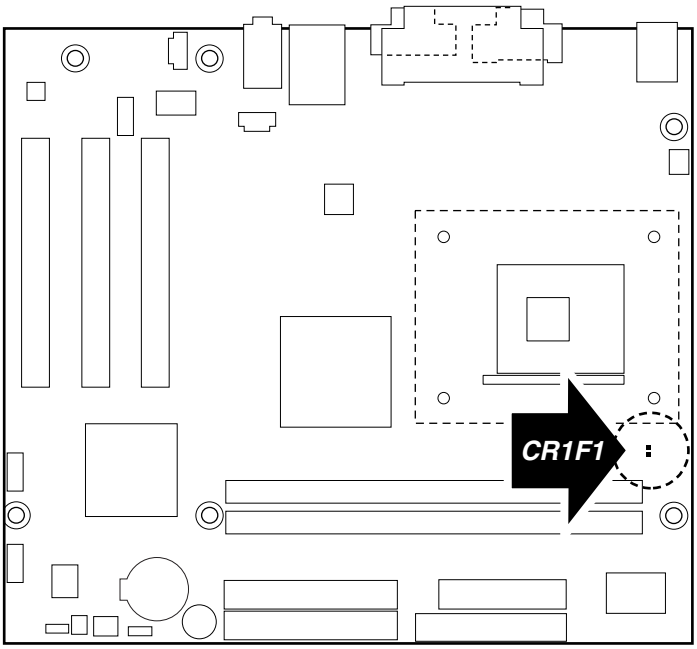


Figure 3. Location of the Standby Power Indicator LED on the D845GVFN Board

1.13.2.6 Resume on Ring

The operation of Resume on Ring can be summarized as follows:

- Resumes operation from ACPI S1 or S3 states
- Detects incoming call similarly for external and internal modems
- Requires modem interrupt be unmasked for correct operation

1.13.2.7 Wake from USB

USB bus activity wakes the computer from ACPI S1 or S3 states.

NOTE

Wake from USB requires the use of a USB peripheral that supports Wake from USB.

1.13.2.8 Wake from PS/2 Devices

PS/2 device activity wakes the computer from an ACPI S1 or S3 state.

1.13.2.9 PME# Signal Wake-up Support

When the PME# signal on the PCI bus is asserted, the computer wakes from an ACPI S1, S3, S4, or S5 state (with Wake on PME enabled in BIOS).

2 Technical Reference

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2.1 Introduction

Sections 2.2 - 2.6 contain several standalone tables. Table 15 describes the system memory map, Table 16 shows the I/O map, Table 17 lists the DMA channels, Table 18 defines the PCI configuration space map, and Table 19 describes the interrupts. The remaining sections in this chapter are introduced by text found with their respective section headings.

2.2 Memory Map

Table 15. System Memory Map

Address Range (decimal)	Address Range (hex)	Size	Description
1024 K - 2097152 K	100000 - 7FFFFFFF	2047 MB	Extended memory
960 K - 1024 K	F0000 - FFFFF	64 KB	Runtime BIOS
896 K - 960 K	E0000 - EFFFF	64 KB	Reserved
800 K - 896 K	C8000 - DFFFF	96 KB	Available high DOS memory (open to the PCI bus)
640 K - 800 K	A0000 - C7FFF	160 KB	Video memory and BIOS
639 K - 640 K	9FC00 - 9FFFF	1 KB	Extended BIOS data (movable by memory manager software)
512 K - 639 K	80000 - 9FBFF	127 KB	Extended conventional memory
0 K - 512 K	00000 - 7FFFF	512 KB	Conventional memory

2.3 Fixed I/O Map

Table 16. I/O Map

Address (hex)	Size	Description
0000 - 00FF	256 bytes	Used by the Desktop Board D845GVFN. Refer to the ICH4 data sheet for dynamic addressing information.
0170 - 0177	8 bytes	Secondary IDE channel
01F0 - 01F7	8 bytes	Primary IDE channel
0228 - 022F (Note 1)	8 bytes	LPT3
0278 - 027F (Note 1)	8 bytes	LPT2
02E8 - 02EF (Note 1)	8 bytes	COM4
02F8 - 02FF (Note 1)	8 bytes	COM2
0376	1 byte	Secondary IDE channel command port
0377, bits 6:0	7 bits	Secondary IDE channel status port
0378 - 037F	8 bytes	LPT1
03B0 - 03BB	12 bytes	Intel 82845GV GMCH
03C0 - 03DF	32 bytes	Intel 82845GV GMCH
03E8 - 03EF	8 bytes	COM3
03F0 - 03F5	6 bytes	Diskette channel 1
03F6	1 byte	Primary IDE channel command port
03F8 - 03FF	8 bytes	COM1
04D0 - 04D1	2 bytes	Edge/level triggered PIC
LPTn + 400	8 bytes	ECP port, LPTn base address + 400h
0CF8 - 0CFB (Note 2)	4 bytes	PCI configuration address register
0CF9 (Note 3)	1 byte	Turbo and reset control register
0CFC - 0CFF	4 bytes	PCI configuration data register
FFA0 - FFA7	8 bytes	Primary bus master IDE registers
FFA8 - FFAF	8 bytes	Secondary bus master IDE registers

Notes:

1. Default, but can be changed to another address range
2. Dword access only
3. Byte access only

NOTE

Some additional I/O addresses are not available due to ICH4 address aliasing. The ICH4 data sheet provides more information on address aliasing.

For information about	Refer to
Obtaining the ICH4 data sheet	Section 1.3 on page 14

2.4 DMA Channels

Table 17. DMA Channels

DMA Channel Number	Data Width	System Resource
0	8 or 16 bits	Open
1	8 or 16 bits	Parallel port
2	8 or 16 bits	Diskette drive
3	8 or 16 bits	Parallel port (for ECP or EPP)
4	8 or 16 bits	DMA controller
5	16 bits	Open
6	16 bits	Open
7	16 bits	Open

2.5 PCI Configuration Space Map

Table 18. PCI Configuration Space Map

Bus Number (hex)	Device Number (hex)	Function Number (hex)	Description
00	00	00	Memory controller of Intel 82845GV component
00	02	00	Intel Extreme Graphics Controller
00	1E	00	Hub link to PCI bridge
00	1F	00	Intel 82801DB ICH4 PCI to LPC bridge
00	1F	01	IDE controller
00	1F	03	SMBus controller
00	1F	05	AC ’97 audio controller
00	1F	06	AC ’97 modem controller (optional)
00	1D	00	USB UHCI controller 1
00	1D	01	USB UHCI controller 2
00	1D	02	USB UHCI controller 3
00	1D	07	EHCI controller
01	08	00	LAN controller (optional)
01	00	00	PCI bus connector 1
01	01	00	PCI bus connector 2
01	02	00	PCI bus connector 3

2.6 Interrupts

The interrupts can be routed through either the Programmable Interrupt Controller (PIC) or the Advanced Programmable Interrupt Controller (APIC) portion of the ICH4 component. The PIC is supported in Windows 98 SE and Windows ME and uses the first 16 interrupts. The APIC is supported in Windows 2000 and Windows XP and supports a total of 24 interrupts.

Table 19. Interrupts

IRQ	System Resource
NMI	I/O channel check
0	Reserved, interval timer
1	Reserved, keyboard buffer full
2	Reserved, cascade interrupt from slave PIC
3	COM2 (Note 1)
4	COM1 (Note 1)
5	LPT2 (Plug and Play option)/User available
6	Diskette drive
7	LPT1 (Note 1)
8	Real-time clock
9	Reserved for ICH4 system management bus
10	User available
11	User available
12	Onboard mouse port (if present, else user available)
13	Reserved, math coprocessor
14	Primary IDE (if present, else user available)
15	Secondary IDE (if present, else user available)
16 (Note 2)	USB UHCI controller 1 (through PIRQA)
17 (Note 2)	AC '97 audio/modem/User available (through PIRQB)
18 (Note 2)	ICH4 USB controller 3 (through PIRQC)
19 (Note 2)	ICH4 USB controller 2 (through PIRQD)
20 (Note 2)	ICH4 LAN (optional) (through PIRQE)
21 (Note 2)	User available (through PIRQF)
22 (Note 2)	User available (through PIRQG)
23 (Note 2)	ICH4 USB 2.0 EHCI controller/User available (through PIRQH)

Notes:

1. Default, but can be changed to another IRQ.
2. Available in APIC mode only.

2.7 PCI Interrupt Routing Map

This section describes interrupt sharing and how the interrupt signals are connected between the PCI bus connectors and onboard PCI devices. The PCI specification specifies how interrupts can be shared between devices attached to the PCI bus. In most cases, the small amount of latency added by interrupt sharing does not affect the operation or throughput of the devices. In some special cases where maximum performance is needed from a device, a PCI device should not share an interrupt with other PCI devices. Use the following information to avoid sharing an interrupt with a PCI add-in card.

PCI devices are categorized as follows to specify their interrupt grouping:

- INTA: By default, all add-in cards that require only one interrupt are in this category. For almost all cards that require more than one interrupt, the first interrupt on the card is also classified as INTA.
- INTB: Generally, the second interrupt on add-in cards that require two or more interrupts is classified as INTB. (This is not an absolute requirement.)
- INTC and INTD: Generally, a third interrupt on add-in cards is classified as INTC and a fourth interrupt is classified as INTD.

The ICH4 has eight Programmable Interrupt Request (PIRQ) input signals. All PCI interrupt sources either onboard or from a PCI add-in card connect to one of these PIRQ signals. Some PCI interrupt sources are electrically tied together on the Desktop Board D845GVFN and therefore share the same interrupt. Table 20 shows an example of how the PIRQ signals are routed.

For example, using Table 20 as a reference, assume an add-in card using INTA is plugged into PCI bus connector 3. In PCI bus connector 3, INTA is connected to PIRQC, which is already connected to the ICH4 USB. The add-in card in PCI bus connector 3 now shares an interrupt with the onboard interrupt source.

Table 20. PCI Interrupt Routing Map

PCI Interrupt Source	ICH4 PIRQ Signal Name							
	PIRQA	**PIRQB**	**PIRQC**	**PIRQD**	**PIRQE**	**PIRQF**	**PIRQG**	**PIRQH**
Intel Extreme Graphics Controller	INTA							
ICH4 USB UHCI controller 1	INTA							
SMBus controller		INTB						
ICH4 USB UHCI controller 2				INTB				
AC '97 ICH4 Audio/Modem		INTB						
ICH4 LAN					INTA			
ICH4 USB UHCI controller 3			INTC					
ICH4 USB 2.0 EHCI controller								INTD
PCI bus connector 1					INTD	INTA	INTB	INTC
PCI bus connector 2					INTC	INTB	INTA	INTD
PCI bus connector 3	INTD	INTC	INTA	INTB				

NOTE

In PIC mode, the ICH4 can connect each PIRQ line internally to one of the IRQ signals (3, 4, 5, 6, 7, 9, 10, 11, 12, 14, and 15). Typically, a device that does not share a PIRQ line will have a unique interrupt. However, in certain interrupt-constrained situations, it is possible for two or more of the PIRQ lines to be connected to the same IRQ signal. Refer to Table 19 for the allocation of PIRQ lines to IRQ signals in APIC mode.

2.8 Connectors

⚠ CAUTION

Only the back panel USB, front panel USB, VGA, and PS/2 connectors have overcurrent protection. The desktop boards' internal connectors are not overcurrent protected and should connect only to devices inside the computer's chassis, such as fans and internal peripherals. Do not use these connectors to power devices external to the computer's chassis. A fault in the load presented by the external devices could cause damage to the computer, the interconnecting cable, and the external devices themselves.

This section describes the board's connectors. The connectors can be divided into these groups:

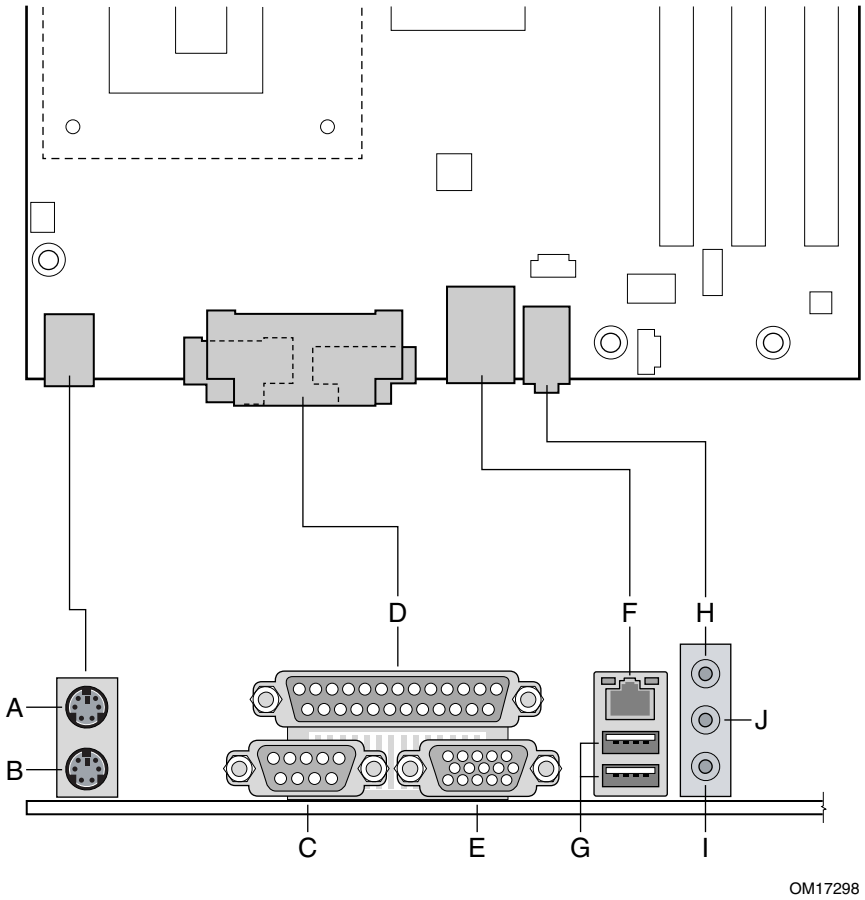
- Back panel I/O connectors (see page 46)
  - PS/2 keyboard and mouse
  - USB (two ports)
  - Parallel port
  - Serial port A
  - VGA port
  - LAN (optional)
  - Audio (line out, line in, and mic in)
- Internal I/O connectors (see page 47)
  - Audio (auxiliary line input, ATAPI CD-ROM, and front panel audio)
  - Fans
  - Power
  - Add-in boards (PCI)
  - IDE
  - Diskette drive
  - Chassis intrusion (optional)
- External I/O connectors (see page 52)
  - Serial Port B (optional)
  - Auxiliary front panel power/sleep LED
  - Front panel (power/sleep LED, power switch, hard drive activity LED, reset switch, and auxiliary front panel power LED)
  - Front panel USB (one connector for two ports)

NOTE

When installing the board in a microATX chassis, make sure that peripheral devices are installed at least 1.5 inches above the main power connector, the diskette drive connector, the IDE connector, and the DIMM sockets.

2.8.1 Back Panel Connectors

Figure 4 shows the location of the back panel connectors. The back panel connectors are color-coded in compliance with PC 99 recommendations. The figure legend below lists the colors used.



Item	Description	Color
A	PS/2 mouse port	Green
B	PS/2 keyboard port	Purple
C	Serial port A	Teal
D	Parallel port	Burgundy
E	VGA	Dark blue
F	LAN (optional)	Black
G	USB ports	Black
H	Audio line in	Light blue
I	Mic in	Pink
J	Audio line out	Lime green

Figure 4. Back Panel Connectors

INTEGRATOR'S NOTE

The back panel audio line out connector is designed to power headphones or amplified speakers only. Poor audio quality occurs if passive (non-amplified) speakers are connected to this output.

2.8.2 Internal I/O Connectors

The internal I/O connectors are divided into the following functional groups:

- Audio, power, and hardware control (see page 48)
  - Front panel audio
  - Auxiliary line in (optional)
  - ATAPI CD-ROM (optional)
  - Fans (3)
  - ATX12V power
  - Main power
  - Chassis intrusion (optional)
- Add-in boards and peripheral interfaces (see page 51)
  - PCI bus
  - IDE
  - Diskette drive

2.8.2.1 Expansion Slots

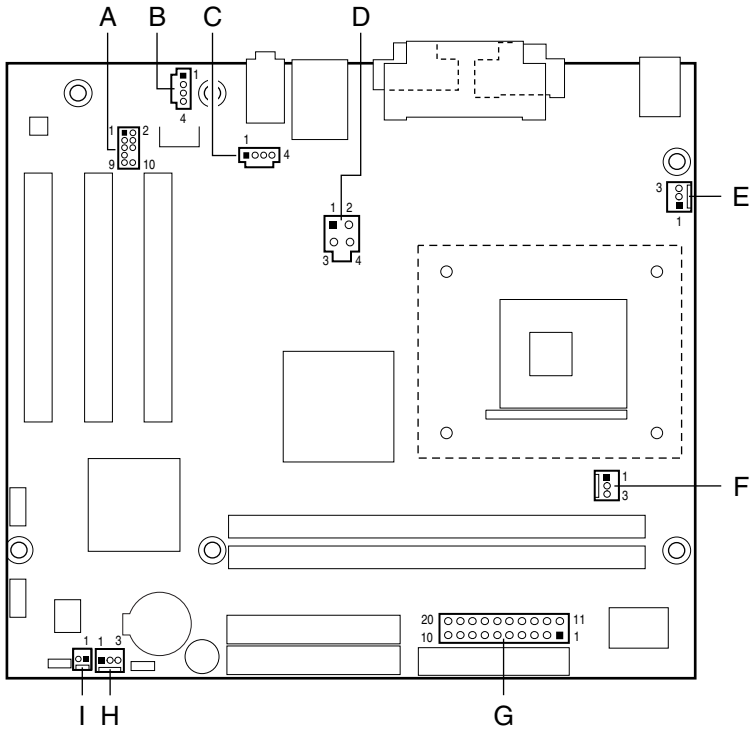
The desktop board has three PCI rev 2.2 compliant local bus slots. The SMBus is routed to PCI bus connector 2.

INTEGRATOR'S NOTE

This document references back-panel slot numbering with respect to processor location on the desktop board. PCI slots are identified as PCI slot #x, starting with the slot closest to the processor. The ATX/microATX specifications identify expansion slot locations with respect to the far edge of a full-sized ATX chassis. The ATX specification and the desktop board's silkscreen are opposite and could cause confusion. The ATX numbering convention is made without respect to slot type, but refers to an actual slot location on a chassis. Figure 6 on page 51 illustrates the desktop board's PCI slot numbering.

2.8.2.2 Audio, Power, and Hardware Control Connectors

Figure 5 shows the location of the audio, power, and hardware control connectors.



Item	Description	For more information see:
A	Front panel audio	Table 21
B	Auxiliary line in, ATAPI style (gray) [optional]	Table 22
C	ATAPI CD-ROM (black) [optional]	Table 23
D	+12 V power connector (ATX12V)	Table 24
E	Rear chassis fan	Table 25
F	Processor fan	Table 26
G	Main power	Table 27
H	Front chassis fan	Table 28
I	Chassis intrusion [optional]	Table 29

Figure 5. Audio, Power, and Hardware Control Connectors

Table 21. Front Panel Audio Connector

Pin	Signal Name	Pin	Signal Name
1	MIC_IN	2	Ground
3	MIC_BIAS	4	+5 V
5	RIGHT_OUT	6	RIGHT_IN
7	No connect	8	Key
9	LEFT_OUT	10	LEFT_IN

Table 22. Auxiliary Line In Connector (Optional)

Pin	Signal Name
1	Left auxiliary line in
2	Ground
3	Ground
4	Right auxiliary line in

Table 23. ATAPI CD-ROM Connector (Optional)

Pin	Signal Name
1	Left audio input from CD-ROM
2	CD audio differential ground
3	CD audio differential ground
4	Right audio input from CD-ROM

INTEGRATOR'S NOTES

- *Use only ATX12V-, SFX12V-, or TFX12V-compliant power supplies with this board. ATX12V, SFX12V, and TFX12V power supplies have an additional power lead that provides required supplemental power for the processor. Always connect the 20-pin and 4-pin leads of ATX12V, SFX12V, and TFX12V power supplies to the corresponding connectors on the desktop board, otherwise the desktop board will not boot.*
- *Do not use a standard ATX power supply. The desktop board will not boot with a standard ATX power supply.*

Table 24. ATX12V Power Connector

Pin	Signal Name	Pin	Signal Name
1	Ground	2	Ground
3	+12 V	4	+12 V

Table 25. Rear Chassis Fan Connector

Pin	Signal Name
1	Ground (default) or FNT_REAR_FAN_CTRL (optional)
2	+12 V
3	No connect (default) or REAR_TACH_OUT (optional)

Table 26. Processor Fan Connector

Pin	Signal Name
1	Ground (default) or CPU_FAN_CTRL (optional)
2	+12 V
3	No connect (default) or CPU_FAN_TACH

Table 27. Main Power Connector

Pin	Signal Name	Pin	Signal Name
1	+3.3 V	11	+3.3 V
2	+3.3 V	12	-12 V
3	Ground	13	Ground
4	+5 V	14	PS-ON# (power supply remote on/off)
5	Ground	15	Ground
6	+5 V	16	Ground
7	Ground	17	Ground
8	PWRGD (Power Good)	18	No connect
9	+5 V (Standby)	19	+5 V
10	+12 V	20	+5 V

Table 28. Front Chassis Fan Connector

Pin	Signal Name
1	Ground (default) or FNT_REAR_FAN_CTRL (optional)
2	+12 V
3	No connect (default) or FRONT_FAN_TACH (optional)

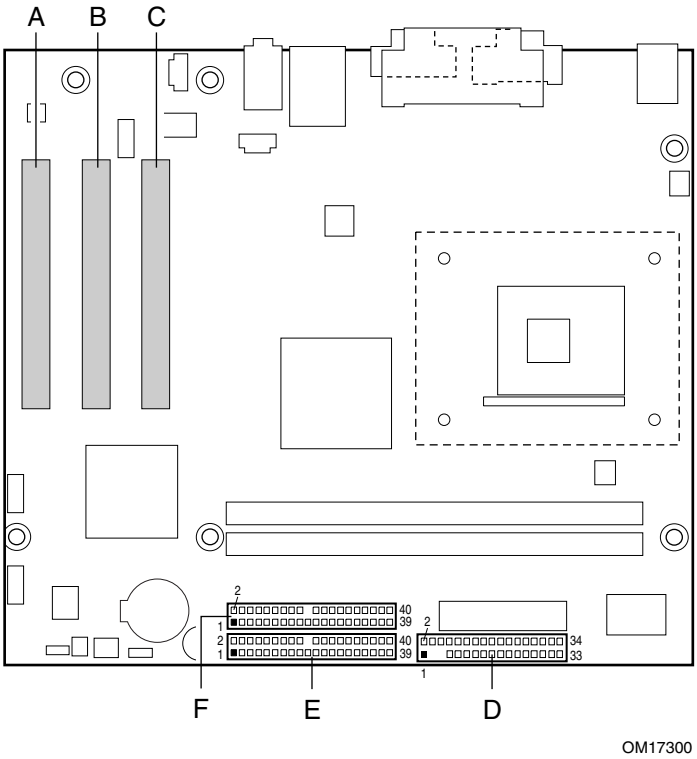
Table 29. Chassis Intrusion Connector (Optional)

Pin	Signal Name
1	Intruder
2	Ground

2.8.2.3 Add-in Board and Peripheral Interface Connectors

Figure 6 shows the location of the add-in board connector and peripheral connectors for the Desktop Board D845GVFN. Note the following considerations for the PCI bus connectors:

- All of the PCI bus connectors are bus master capable.
- SMBus signals are routed to PCI bus connector 2, enabling PCI bus add-in boards with SMBus support to access sensor data on the desktop board. The SMBus signals are as follows:
  - The SMBus clock line is connected to pin A40.
  - The SMBus data line is connected to pin A41.

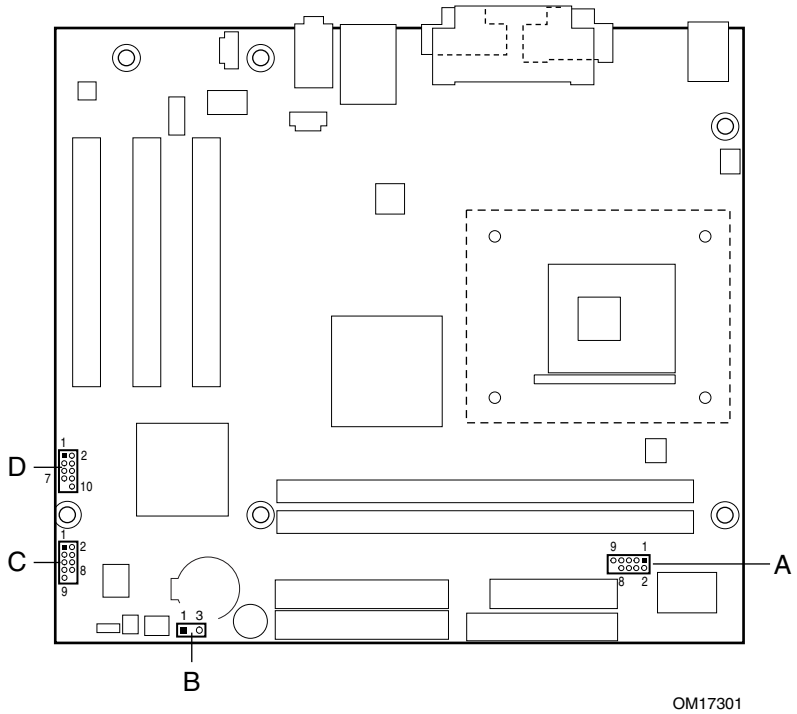


Item	Description
A	PCI bus connector 3
B	PCI bus connector 2
C	PCI bus connector 1
D	Diskette drive
E	Primary IDE
F	Secondary IDE

Figure 6. Add-in Board and Peripheral Interface Connectors

2.8.3 External I/O Connectors

Figure 7 shows the locations of the external I/O connectors.



Item	Description	For more information see:
A	Serial Port B (optional)	Table 30
B	Auxiliary front panel power/sleep LED	Table 31
C	Front panel	Table 32 and Figure 8
D	Front panel USB	Figure 9

Figure 7. External I/O Connectors

Table 30. Serial Port B Connector (optional)

Pin	Signal Name	Pin	Signal Name
1	DCD	2	RXD
3	TXD	4	DTR
5	Ground	6	DSR
7	RTS	8	CTS
9	RI	10	Not connected

2.8.3.1 Auxiliary Front Panel Power/Sleep LED Connector

Pins 1 and 3 of this connector duplicate the signals on pins 2 and 4 of the front panel connector. Table 31 lists the signal names of the Auxiliary Front Panel Power/Sleep LED Connector.

Table 31. Auxiliary Front Panel Power/Sleep LED Connector

Pin	Signal Name	In/Out	Description
1	HDR_BLNK_GRN	Out	Front panel green LED
2	Not connected		
3	HDR_BLNK_YEL	Out	Front panel yellow LED

2.8.3.2 Front Panel Connector

This section describes the functions of the front panel connector. Table 32 lists the signal names of the front panel connector. Figure 8 is a connection diagram for the front panel connector.

Table 32. Front Panel Connector

Pin	Signal	In/Out	Description	Pin	Signal	In/Out	Description
Hard Drive Activity LED				**Power LED**			
1	HD_PWR	Out	Hard disk LED pull-up (750 Ω) to +5 V	2	HDR_BLNK_ GRN	Out	Front panel green LED
3	HAD#	Out	Hard disk active LED	4	HDR_BLNK_ YEL	Out	Front panel yellow LED
Reset Switch				**On/Off Switch**			
5	Ground		Ground	6	SWITCH_ON#	In	Power switch
7	FP_RESET#	In	Reset switch	8	Ground		Ground
9	+5 V	Out	Power	10	No connect		Not connected

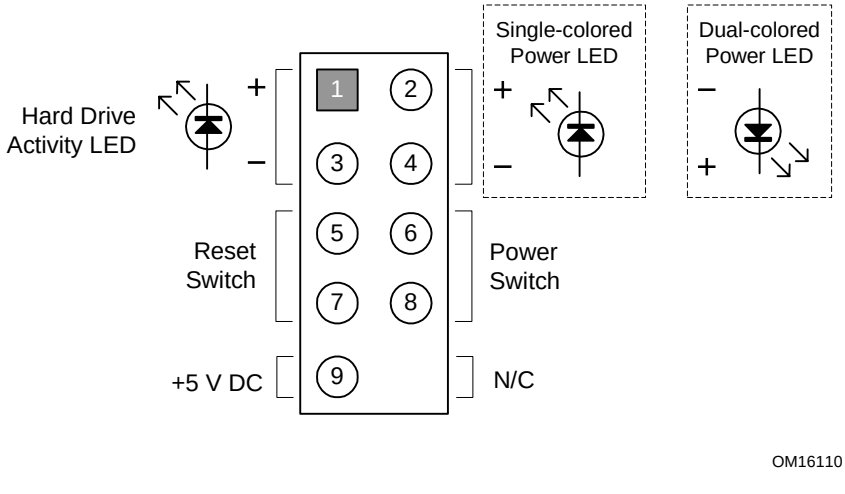


Figure 8. Connection Diagram for Front Panel Connector

2.8.3.2.1 Hard Drive Activity LED Connector

Pins 1 and 3 can be connected to an LED to provide a visual indicator that data is being read from or written to a hard drive. For the LED to function properly, an IDE drive must be connected to the onboard IDE interface.

2.8.3.2.2 Reset Switch Connector

Pins 5 and 7 can be connected to a momentary SPST type switch that is normally open. When the switch is closed, the desktop board resets and runs the POST.

2.8.3.2.3 Power/Sleep LED Connector

Pins 2 and 4 can be connected to a one- or two-color LED. Table 33 shows the possible states for a one-color LED. Table 34 shows the possible states for a two-color LED.

Table 33. States for a One-Color Power LED

LED State	Description
Off	Power off/sleeping
Steady Green	Running

Table 34. States for a Two-Color Power LED

LED State	Description
Off	Power off
Steady Green	Running
Steady Yellow	Sleeping

NOTE

The colors listed in Table 33 and Table 34 are suggested colors only. Actual LED colors are product- or customer-specific.

2.8.3.2.4 Power Switch Connector

Pins 6 and 8 can be connected to a front panel momentary-contact power switch. The switch must pull the SW_ON# pin to ground for at least 50 ms to signal the power supply to switch on or off. (The time requirement is due to internal debounce circuitry on the Desktop Board D845GVFN.) At least two seconds must pass before the power supply will recognize another on/off signal.

2.8.3.3 Front Panel USB Connector

Figure 9 is a connection diagram for the front panel USB connector.

INTEGRATOR'S NOTES

- *The +5 V DC power on the USB connector is fused.*
- *Pins 1, 3, 5, and 7 comprise one USB port.*
- *Pins 2, 4, 6, and 8 comprise one USB port.*
- *Use only a front panel USB connector that conforms to the USB 2.0 specification for high-speed USB devices.*

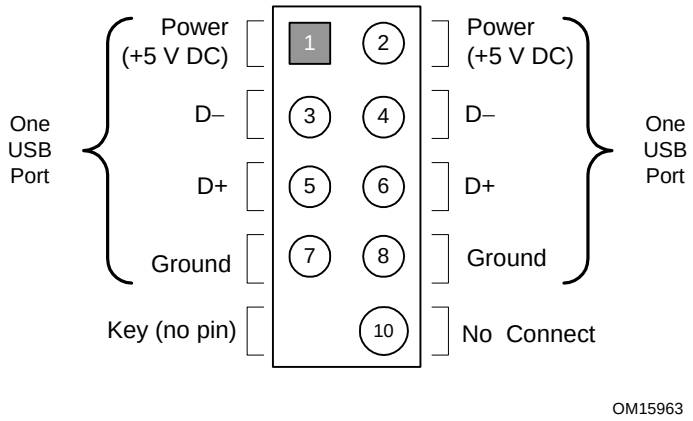


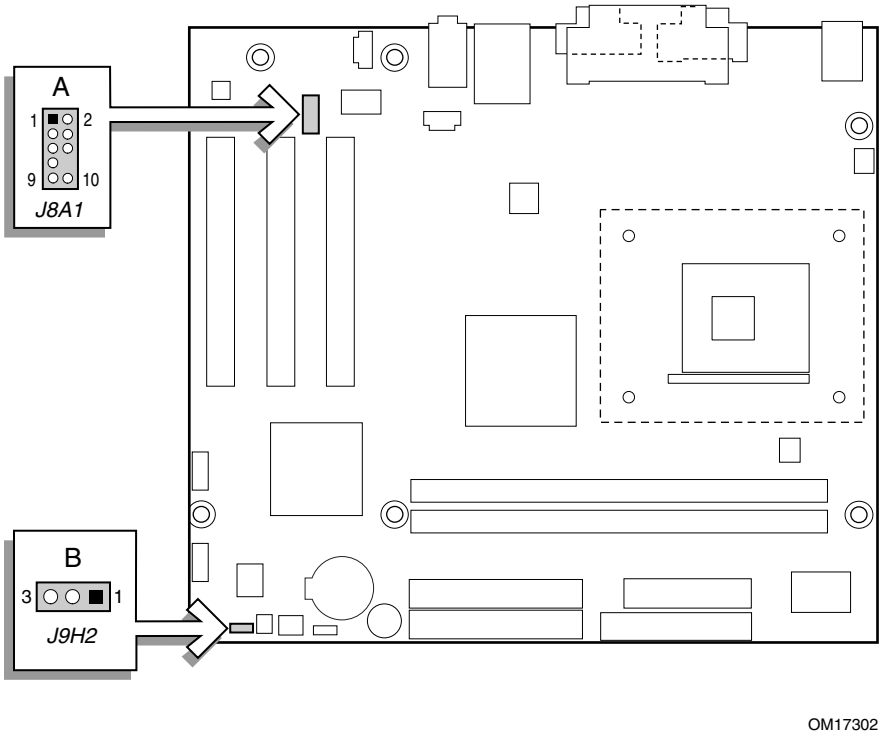
Figure 9. Connection Diagram for Front Panel USB Connector

2.9 Jumper Blocks

CAUTION

Do not move any jumpers with the power on. Always turn off the power and unplug the power cord from the computer before changing a jumper setting. Otherwise, the desktop board could be damaged.

Figure 10 shows the location of the jumper blocks.



Item	Description	Reference Designator
A	Front panel audio connector/jumper block	J8A1
B	BIOS Setup configuration jumper block	J9H2

Figure 10. Location of the Jumper Blocks

2.9.1 Front Panel Audio Connector/Jumper Block

This connector has two functions:

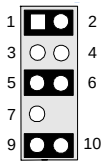
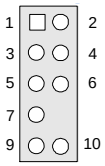
- With jumpers installed, the audio line out signals are routed to the back panel audio line out connector.
- With jumpers removed, the connector provides audio line out and mic in signals for front panel audio connectors.

Table 35 describes the two configurations of this connector/jumper block.

CAUTION

Do not place jumpers on this block in any configuration other than the one described in Table 35. Other jumper configurations are not supported and could damage the desktop board.

Table 35. Front Panel Audio Connector/Jumper Block

Jumper Setting		Configuration
	1 and 2 5 and 6 9 and 10	Audio line out signals are routed to the back panel audio line out connector. The back panel audio line out connector is shown in Figure 4 on page 46.
	No jumpers installed	Audio line out and mic in signals are available for front panel audio connectors. Table 21 on page 49 lists the names of the signals available on this connector when no jumpers are installed.

INTEGRATOR'S NOTE

When the jumpers are removed and this connector is used for front panel audio, the back panel audio line out and mic in connectors are disabled.

2.9.2 BIOS Setup Configuration Jumper Block

The 3-pin jumper block determines the BIOS Setup program's mode. Table 36 describes the jumper settings for the three modes: normal, configure, and recovery. When the jumper is set to configuration mode and the computer is powered-up, the BIOS compares the processor version and the microcode version in the BIOS and reports if the two match.

Table 36. BIOS Setup Configuration Jumper Settings

Function/Mode	Jumper Setting		Configuration
Normal	1-2		The BIOS uses current configuration information and passwords for booting.
Configure	2-3		After the POST runs, Setup runs automatically. The maintenance menu is displayed.
Recovery	None		The BIOS attempts to recover the BIOS configuration. A recovery diskette is required.

2.10 Mechanical Considerations

The Desktop Board D845GVFN is designed to fit into either a microATX or an ATX-form-factor chassis. Figure 11 illustrates the mechanical form factor for the desktop board. Dimensions are given in inches [millimeters]. The outer dimensions are 9.20 inches by 8.20 inches [233.68 millimeters by 208.28 millimeters]. Location of the I/O connectors and mounting holes are in compliance with the ATX specification.

INTEGRATOR'S NOTE

When installing the desktop board in a microATX chassis, make sure that peripheral devices are installed at least 1.5 inches above the main power connector, the diskette drive connector, the IDE connector, and the DIMM sockets.

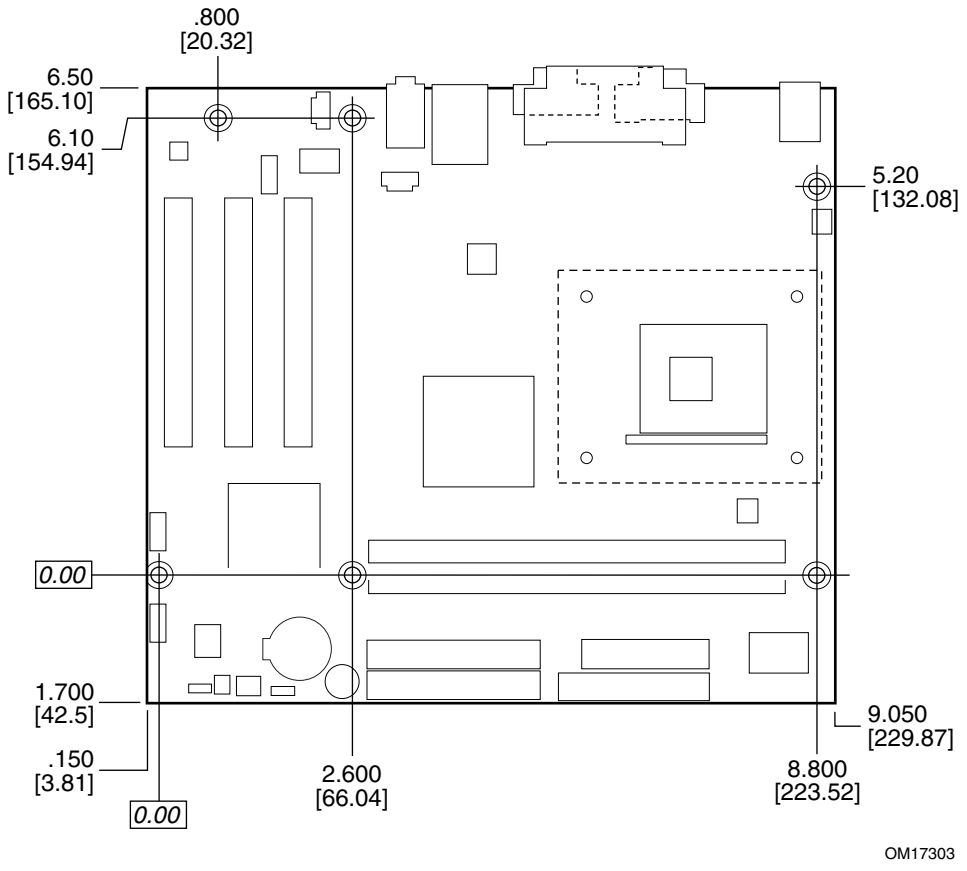


Figure 11. Desktop Board Dimensions

2.10.1 I/O Shield

The back panel I/O shield for the Desktop Board D845GVFN must meet specific dimension and material requirements. Systems based on this desktop board need the back panel I/O shield to pass emissions (EMI) certification testing. Figure 12 shows the critical dimensions of the I/O shield. Dimensions are given in inches [millimeters], to a tolerance of ±0.020 inches [0.508 millimeters].

The figures also indicate the position of each cutout. Additional design considerations for I/O shields relative to chassis requirements are described in the ATX specification. See Section 1.5 for information about the ATX specification.

INTEGRATOR'S NOTE

An I/O shield compliant with the ATX chassis specification 2.03 is available from Intel.

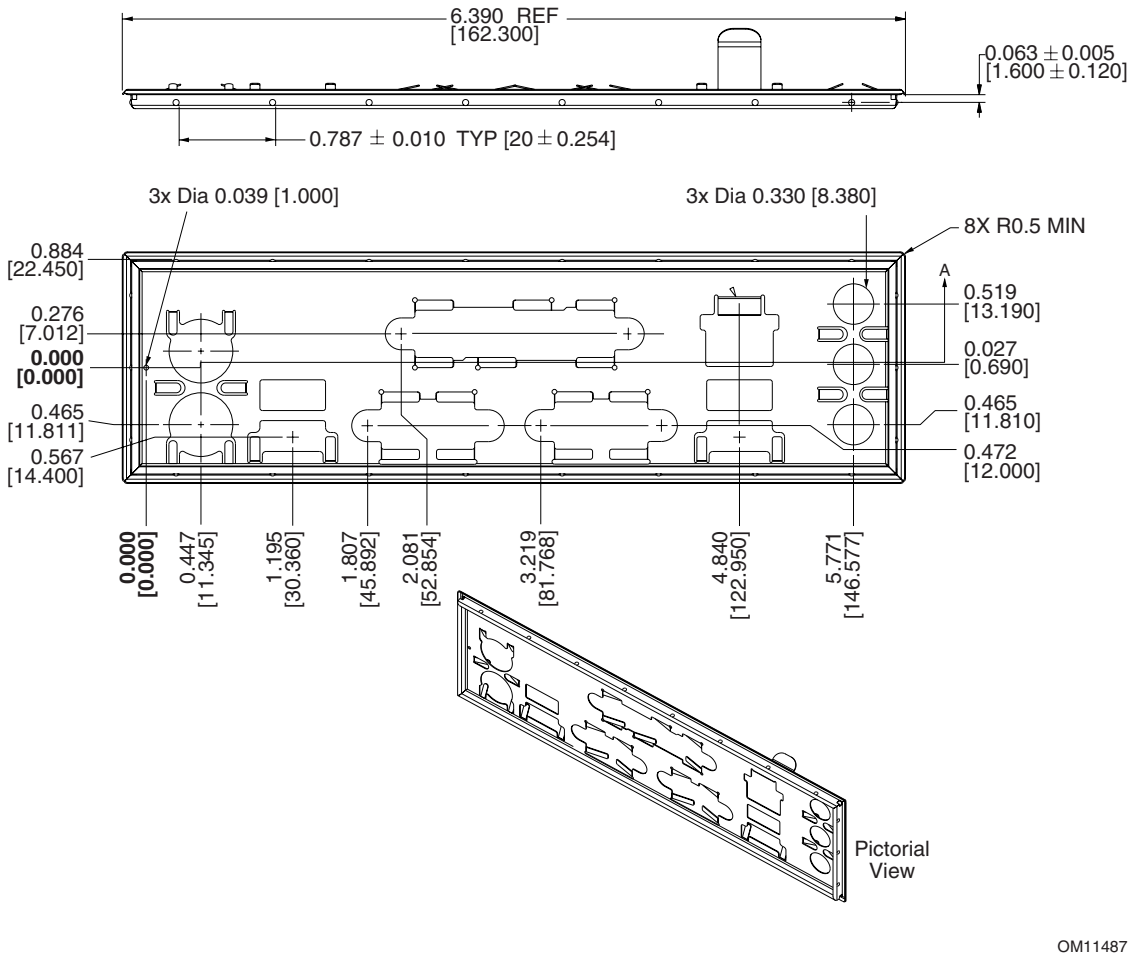


Figure 12. I/O Shield Dimensions

2.11 Electrical Considerations

2.11.1 DC Loading

Table 37 lists the DC loading characteristics of the board. This data is based on a DC analysis of all active components within the board that impact its power delivery subsystems. The analysis does not include PCI add-in cards. Minimum values assume a light load placed on the board that is similar to an environment with no applications running and no USB current draw. Maximum values assume a load placed on the board that is similar to a heavy gaming environment with a 500 mA current draw per USB port. These calculations are not based on specific processor values or memory configurations but are based on the minimum and maximum current draw possible from the board's power delivery subsystems to the processor, memory, and USB ports.

Use the datasheets for add-in cards, such as PCI, to determine the overall system power requirements. The selection of a power supply at the system level is dependent on the system's usage model and not necessarily tied to a particular processor speed.

Table 37. DC Loading Characteristics

		DC Current at:				
Mode	**DC Power**	**+3.3 V**	**+5 V**	**+12 V**	**-12 V**	**+5 VSB**
Minimum loading	190.00 W	5.00 A	11.00 A	9.00 A	0.03 A	0.60 A
Maximum loading	286.00 W	11.00 A	15.00 A	13.00 A	0.10 A	1.40 A

2.11.2 Add-in Board Considerations

The Desktop Board D845GVFN is designed to provide 2 A (average) of +5 V current for each add-in board. The total +5 V current draw for add-in boards for a fully loaded Desktop Board D845GVFN (all three expansion slots filled) must not exceed 6 A.

2.11.3 Fan Connector Current Capability

⚠ CAUTION

The processor fan must be connected to the processor fan connector, not to a chassis fan connector. Connecting the processor fan to a chassis fan connector may result in onboard component damage that will halt fan operation.

Table 38 lists the current capability of the fan connectors on the Desktop Board D845GVFN.

Table 38. Fan Connector Current Capability

Fan Connector	Maximum Available Current
Processor fan	1.00 A
Front chassis fan	1.00 A
Rear chassis fan	1.00 A

2.11.4 Power Supply Considerations

CAUTION

The +5 V standby line for the power supply must be capable of providing adequate +5 V standby current. Failure to do so can damage the power supply. The total amount of standby current required depends on the wake devices supported and manufacturing options.

System integrators should refer to the power usage values listed in Table 37 when selecting a power supply for use with the Desktop Board D845GVFN.

Additional power required will depend on configurations chosen by the integrator.

The power supply must comply with the following recommendations found in the indicated sections of the ATX form factor specification.

- The potential relation between 3.3 VDC and +5 VDC power rails (Section 4.2)
- The current capability of the +5 VSB line (Section 4.2.1.2)
- All timing parameters (Section 4.2.1.3)
- All voltage tolerances (Section 4.2.2)

For information about	Refer to
The ATX form factor specification	Section 1.5, page 15

2.12 Thermal Considerations

CAUTION

The use of an Intel Pentium 4 processor operating above 2.80 GHz with this Intel desktop board requires the following:

- *A chassis with appropriate airflow to ensure proper cooling of the components on the board*
- *A processor fan heatsink that meets the thermal performance targets for Pentium 4 processors operating above 2.80 GHz*

Failure to ensure appropriate airflow may result in reduced performance of both the processor and/or voltage regulator or, in some instances, damage to the desktop board. For a list of chassis that have been tested with Intel desktop boards please refer to the following website:

http://developer.intel.com/design/motherbd/cooling.htm

All responsibility for determining the adequacy of any thermal or system design remains solely with the reader. Intel makes no warranties or representations that merely following the instructions presented in this document will result in a system with adequate thermal performance.

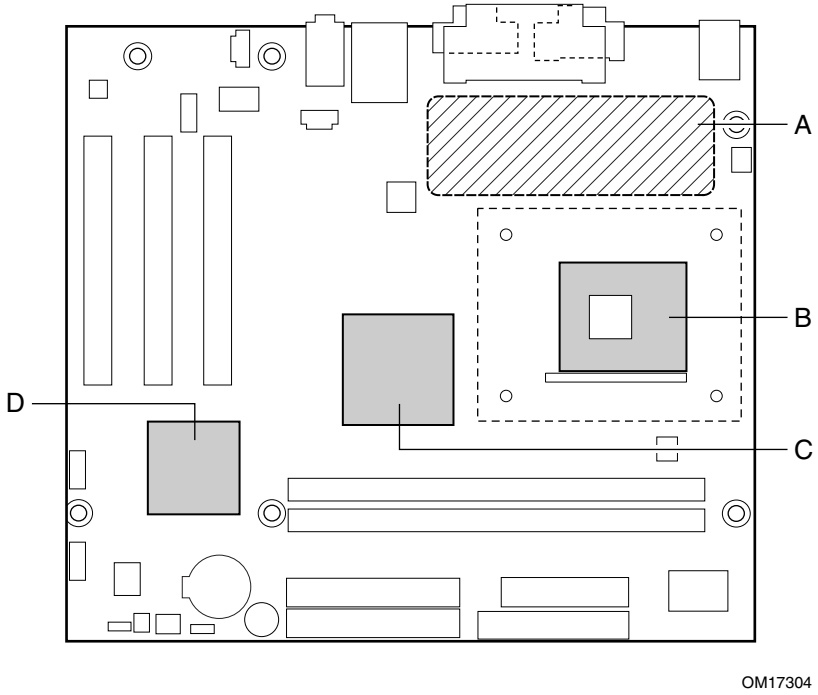
CAUTION

Ensure that the ambient temperature does not exceed the desktop board's maximum operating temperature. Failure to do so could cause components to exceed their maximum case temperature and malfunction. For information about the maximum operating temperature, see the environmental specifications in Section 2.14.

⚠ CAUTION

Ensure that proper airflow is maintained in the processor voltage regulator circuit. Failure to do so may result in damage to the voltage regulator circuit. The processor voltage regulator area (item A in Figure 13) can reach a temperature of up to 85 °C in an open chassis.

Figure 13 shows the locations of the localized high temperature zones.



Item	Description
A	Processor voltage regulator area
B	Processor
C	Intel 82845GV GMCH
D	Intel 82801DB ICH4

Figure 13. Localized High Temperature Zones

Table 39 provides maximum case temperatures for Desktop Board D845GVFN components that are sensitive to thermal changes. The operating temperature, current load, or operating frequency could affect case temperatures. Maximum case temperatures are important when considering proper airflow to cool the Desktop Board D845GVFN.

Table 39. Thermal Considerations for Components

Component	Maximum Case Temperature
Intel Pentium 4 processor	For processor case temperature, see processor datasheets and processor specification updates
Intel 82845GV GMCH	92 °C (under bias)
Intel 82801DB ICH4	110 °C (under bias)

2.13 Reliability

The Mean Time Between Failures (MTBF) prediction is calculated using component and subassembly random failure rates. The calculation is based on the Bellcore Reliability Prediction Procedure, TR-NWT-000332, Issue 4, September 1991. The MTBF prediction is used to estimate repair rates and spare parts requirements.

The MTBF data is calculated from predicted data at 55 ºC. The Desktop Board D845GVFN MTBF is 149979.68 hours.

2.14 Environmental

Table 40 lists the environmental specifications for the Desktop Board D845GVFN.

Table 40. Desktop Board D845GVFN Environmental Specifications

Parameter	Specification		
Temperature			
Non-Operating	-40 °C to +70 °C		
Operating	0 °C to +55 °C		
Shock			
Unpackaged	50 g trapezoidal waveform		
	Velocity change of 170 inches/second		
Packaged	Half sine 2 millisecond		
	Product Weight (pounds)	Free Fall (inches)	Velocity Change (inches/sec)
	<20	36	167
	21-40	30	152
	41-80	24	136
	81-100	18	118
Vibration			
Unpackaged	5 Hz to 20 Hz: 0.01 g^2 Hz sloping up to 0.02 g^2 Hz		
	20 Hz to 500 Hz: 0.02 g^2 Hz (flat)		
Packaged	10 Hz to 40 Hz: 0.015 g^2 Hz (flat)		
	40 Hz to 500 Hz: 0.015 g^2 Hz sloping down to 0.00015 g^2 Hz		

2.15 Regulatory Compliance

This section describes the desktop boards' compliance with U.S. and international safety and electromagnetic compatibility (EMC) regulations.

2.15.1 Safety Regulations

Table 41 lists the safety regulations the Desktop Board D845GVFN complies with when correctly installed in a compatible host system.

Table 41. Safety Regulations

Regulation	Title
UL 60950 3rd ed., 2000/CSA C22.2 No. 60950-00	Bi-National Standard for Safety of Information Technology Equipment including Electrical Business Equipment. (USA and Canada)
EN 60950:2000	The Standard for Safety of Information Technology Equipment including Electrical Business Equipment. (European Union)
IEC 60950, 3rd Edition, 1999	The Standard for Safety of Information Technology Equipment including Electrical Business Equipment. (International)

2.15.2 EMC Regulations

Table 42 lists the EMC regulations the Desktop Board D845GVFN complies with when correctly installed in a compatible host system.

Table 42. EMC Regulations

Regulation	Title
FCC (Class B)	Title 47 of the Code of Federal Regulations, Parts 2 and 15, Subpart B, Radio Frequency Devices. (USA)
ICES-003 (Class B)	Interference-Causing Equipment Standard, Digital Apparatus. (Canada)
EN55022: 1998 (Class B)	Limits and methods of measurement of Radio Interference Characteristics of Information Technology Equipment. (European Union)
EN55024: 1998	Information Technology Equipment – Immunity Characteristics Limits and methods of measurement. (European Union)
AS/NZS 3548 (Class B)	Australian Communications Authority, Standard for Electromagnetic Compatibility. (Australia and New Zealand)
CISPR 22, 3rd Edition (Class B)	Limits and methods of measurement of Radio Disturbance Characteristics of Information Technology Equipment. (International)
CISPR 24: 1997	Information Technology Equipment – Immunity Characteristics – Limits and Methods of Measurements. (International)

2.15.2.1 FCC Compliance Statement (USA)

Product Type: D845GVFN Desktop Board

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and the receiver.
- Connect the equipment to a different electrical branch circuit from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Any changes or modifications to the equipment not expressly approved by Intel Corporation could void the user's authority to operate the equipment.

2.15.2.2 Canadian Compliance Statement

This Class B digital apparatus complies with Canadian ICES-003.

Cet appereil numérique de la classe B est conforme à la norme NMB-003 du Canada.

2.15.3 European Union Declaration of Conformity Statement

We, Intel Corporation, declare under our sole responsibility that the product: Intel® Desktop Board D845GVFN is in conformity with all applicable essential requirements necessary for CE marking, following the provisions of the European Council Directive 89/336/EEC (EMC Directive) and Council Directive 73/23/EEC (Safety/Low Voltage Directive).

The product is properly CE marked demonstrating this conformity and is for distribution within all member states of the EU with no restrictions.

CE

This product follows the provisions of the European Directives 89/336/EEC and 73/23/EEC.

2.15.4 Product Ecology Statements

The following information is provided to address worldwide product ecology concerns and regulations.

2.15.4.1 Disposal Considerations

This product contains the following materials that may be regulated upon disposal: lead solder on the printed wiring board assembly.

2.15.4.2 Recycling Considerations

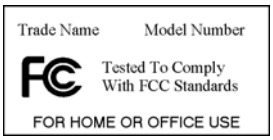
Intel encourages its customers to recycle its products and their components (e.g., batteries, circuit boards, plastic enclosures, etc.) whenever possible. In the U.S., a list of recyclers in your area can be found at:
http://www.eiae.org/

In the absence of a viable recycling option, products and their components must be disposed of in accordance with all applicable local environmental regulations.

2.15.5 Product Certification Markings (Board Level)

Table 43 lists the board's product certification markings.

Table 43. Product Certification Markings

Description	Marking
UL joint US/Canada Recognized Component mark. Includes adjacent UL file number for Intel Desktop Boards: E210882 (component side).	
FCC Declaration of Conformity logo mark for Class B equipment; includes Intel name and D845GVFN model designation (component side).	
CE mark. Declares compliance to European Union (EU) EMC directive (89/336/EEC) and Low Voltage directive (73/23/EEC) (component side). The CE mark should also be on the shipping container.	
Australian Communications Authority (ACA) C-Tick mark. Includes adjacent Intel supplier code number, N-232. The C-tick mark should also be on the shipping container.	
Printed wiring board manufacturer's recognition mark: consists of a unique UL recognized manufacturer's logo, along with a flammability rating (solder side).	94V-0

3 Overview of BIOS Features

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3.1 Introduction

The board uses an Intel/AMI BIOS that is stored in the Firmware Hub (FWH) and can be updated using a disk-based program. The FWH contains the BIOS Setup program, POST, the PCI auto-configuration utility, and Plug and Play support.

The BIOS displays a message during POST identifying the type of BIOS and a revision code. The initial production BIOSs are identified as FN84510A.86A.

When the BIOS Setup program configuration jumper is set to configuration mode and the computer is powered-up, the BIOS compares the CPU version and the microcode version in the BIOS and reports if the two match.

The BIOS Setup program can be used to view and change the BIOS settings for the computer. The BIOS Setup program is accessed by pressing the <F2> key after the Power-On Self-Test (POST) memory test begins and before the operating system boot begins. The menu bar is shown below.

Maintenance	Main	Advanced	Security	Power	Boot	Exit

NOTE

The maintenance menu is displayed only when the board is in configuration mode. Section 2.9.2 on page 57 tells how to put the board in configuration mode.

Table 44 lists the BIOS Setup program menu features.

Table 44. BIOS Setup Program Menu Bar

Maintenance	Main	Advanced	Security	Power	Boot	Exit
Clears passwords and BIS credentials and enables extended configuration mode	Allocates resources for hardware components	Configures advanced features available through the chipset	Sets passwords and security features	Configures power management features	Selects boot options and power supply controls	Saves or discards changes to Setup program options

Table 45 lists the function keys available for menu screens.

Table 45. BIOS Setup Program Function Keys

BIOS Setup Program Function Key	Description
<←> or <→>	Selects a different menu screen (Moves the cursor left or right)
<↑> or <↓>	Selects an item (Moves the cursor up or down)
<Tab>	Selects a field (Not implemented)
<Enter>	Executes command or selects the submenu
<F9>	Load the default configuration values for the current menu
<F10>	Save the current values and exits the BIOS Setup program
<Esc>	Exits the menu

For information about	Refer to
The desktop boards' compliance level with Plug and Play	Section 1.5, page 15

3.2 BIOS Flash Memory Organization

The Firmware Hub (FWH) includes a 3 Mbit (384 KB) symmetrical flash memory device.

3.3 Resource Configuration

3.3.1 PCI Autoconfiguration

The BIOS can automatically configure PCI devices. PCI devices may be onboard or add-in cards. Autoconfiguration lets a user insert or remove PCI cards without having to configure the system. When a user turns on the system after adding a PCI card, the BIOS automatically configures interrupts, the I/O space, and other system resources. Any interrupts set to Available in Setup are considered to be available for use by the add-in card.

For information about the versions of PCI and Plug and Play supported by the BIOS, see Section 1.5.

3.3.2 PCI IDE Support

If you select Auto in the BIOS Setup program, the BIOS automatically sets up the two PCI IDE connectors with independent I/O channel support. The IDE interface supports hard drives up to ATA-66/100 and recognizes any ATAPI compliant devices, including CD-ROM drives, tape drives, and Ultra DMA drives (see Section 1.5 for the supported version of ATAPI). The BIOS determines the capabilities of each drive and configures them to optimize capacity and performance. To take advantage of the high capacities typically available today, hard drives are automatically configured for Logical Block Addressing (LBA) and to PIO Mode 3 or 4, depending on the capability of the drive. You can override the auto-configuration options by specifying manual configuration in the BIOS Setup program.

To use ATA-66/100 features the following items are required:

- An ATA-66/100 peripheral device
- An ATA-66/100 compatible cable
- ATA-66/100 operating system device drivers

NOTE

ATA-66/100 compatible cables are backward compatible with drives using slower IDE transfer protocols. If an ATA-66/100 disk drive and a disk drive using any other IDE transfer protocol are attached to the same cable, the maximum transfer rate between the drives is reduced to that of the slowest device.

NOTE

Do not connect an ATA device as a slave on the same IDE cable as an ATAPI master device. For example, do not connect an ATA hard drive as a slave to an ATAPI CD-ROM drive.

3.4 System Management BIOS (SMBIOS)

SMBIOS is a Desktop Management Interface (DMI) compliant method for managing computers in a managed network.

The main component of SMBIOS is the Management Information Format (MIF) database, which contains information about the computing system and its components. Using SMBIOS, a system administrator can obtain the system types, capabilities, operational status, and installation dates for system components. The MIF database defines the data and provides the method for accessing this information. The BIOS enables applications such as third-party management software to use SMBIOS. The BIOS stores and reports the following SMBIOS information:

- BIOS data, such as the BIOS revision level
- Fixed-system data, such as peripherals, serial numbers, and asset tags
- Resource data, such as memory size, cache size, and processor speed
- Dynamic data, such as event detection and error logging

Non-Plug and Play operating systems, such as Windows NT*, require an additional interface for obtaining the SMBIOS information. The BIOS supports an SMBIOS table interface for such operating systems. Using this support, an SMBIOS service-level application running on a non-Plug and Play operating system can obtain the SMBIOS information.

For information about	Refer to
The desktop boards' compliance level with SMBIOS	Section 1.5, page 15

3.5 Legacy USB Support

Legacy USB support enables USB devices such as keyboards, mice, and hubs to be used even when the operating system's USB drivers are not yet available. Legacy USB support is used to access the BIOS Setup program, and to install an operating system that supports USB. By default, Legacy USB support is set to Enabled.

Legacy USB support operates as follows:

1. When you apply power to the computer, legacy support is disabled.
2. POST begins.
3. Legacy USB support is enabled by the BIOS allowing you to use a USB keyboard to enter and configure the BIOS Setup program and the maintenance menu.
4. POST completes.
5. The operating system loads. While the operating system is loading, USB keyboards and mice are recognized and may be used to configure the operating system. (Keyboards and mice are not recognized during this period if Legacy USB support was set to Disabled in the BIOS Setup program.)
6. After the operating system loads the USB drivers, all legacy and non-legacy USB devices are recognized by the operating system, and Legacy USB support from the BIOS is no longer used.

To install an operating system that supports USB, verify that Legacy USB support in the BIOS Setup program is set to Enabled and follow the operating system's installation instructions.

3.6 BIOS Updates

The BIOS can be updated using either of the following utilities, which are available on the Intel World Wide Web site:

- Intel® Express BIOS Update utility, which enables automated updating while in the Windows environment. Using this utility, the BIOS can be updated from a file on a hard disk, a 1.44 MB diskette, or a CD-ROM, or from the file location on the Web.
- Intel® Flash Memory Update Utility, which requires creation of a boot diskette and manual rebooting of the system. Using this utility, the BIOS can be updated from a file on a 1.44 MB diskette (from a legacy diskette drive or an LS-120 diskette drive) or a CD-ROM.

Both utilities Verifying that the updated BIOS matches the target system to prevent accidentally installing an incompatible BIOS.

NOTE

Review the instructions distributed with the upgrade utility before attempting a BIOS update.

For information about	Refer to
The Intel World Wide Web site	Section 1.3, page 14

3.6.1 Language Support

The BIOS Setup program and help messages are supported in five languages: US English, German, Italian, French, and Spanish. The default language is US English, which is present unless another language is selected in the BIOS Setup program.

3.6.2 Custom Splash Screen

During POST, an Intel splash screen is displayed by default. This splash screen can be replaced with a custom splash screen. The Integrator's Toolkit that is available from Intel can be used to create a custom splash screen.

NOTE

If you add a custom splash screen, it will share space with the Intel branded logo.

For information about	Refer to
The Intel World Wide Web site	Section 1.3, page 14

3.7 Boot Options

In the BIOS Setup program, the user can choose to boot from a diskette drive, hard drives, CD-ROM, or the network. The default setting is for the diskette drive to be the first boot device, the hard drive second, and the ATAPI CD-ROM third. The fourth device is disabled.

3.7.1 CD-ROM Boot

Booting from CD-ROM is supported in compliance to the El Torito bootable CD-ROM format specification. Under the Boot menu in the BIOS Setup program, ATAPI CD-ROM is listed as a boot device. Boot devices are defined in priority order. Accordingly, if there is not a bootable CD in the CD-ROM drive, the system will attempt to boot from the next defined drive.

For information about	Refer to
The El Torito specification	Section 1.5, page 15

3.7.2 Network Boot

The network can be selected as a boot device. This selection allows booting from the onboard LAN or a network add-in card with a remote boot ROM installed.

Pressing the <F12> key during POST automatically forces boot from the LAN.

3.7.3 Booting Without Attached Devices

For use in embedded applications, the BIOS has been designed so that after passing the POST, the operating system loader is invoked even if the following devices are not present:

- Video adapter
- Keyboard
- Mouse

3.7.4 Changing the Default Boot Device During POST

Pressing the <F10> key during POST causes a boot device menu to be displayed. This menu displays the list of available boot devices (as set in the BIOS setup program's Boot Device Priority Submenu). Table 46 lists the boot device menu options.

Table 46. Boot Device Menu Options

Boot Device Menu Function Keys	Description
<↑> or <↓>	Selects a default boot device
<Enter>	Exits the menu, saves changes, and boots from the selected device
<Esc>	Exits the menu without saving changes

3.8 Fast Booting Systems with Intel® Rapid BIOS Boot

These factors affect system boot speed:

- Selecting and configuring peripherals properly
- Using an optimized BIOS, such as the Intel® Rapid BIOS

3.8.1 Peripheral Selection and Configuration

The following techniques help improve system boot speed:

- Choose a hard drive with parameters such as “power-up to data ready” less than eight seconds, that minimize hard drive startup delays.
- Select a CD-ROM drive with a fast initialization rate. This rate can influence POST execution time.
- Eliminate unnecessary add-in adapter features, such as logo displays, screen repaints, or mode changes in POST. These features may add time to the boot process.
- Try different monitors. Some monitors initialize and communicate with the BIOS more quickly, which enables the system to boot more quickly.

3.8.2 Intel Rapid BIOS Boot

Use of the following BIOS Setup program settings reduces the POST execution time.

In the Boot Menu:

- Set the hard disk drive as the first boot device. As a result, the POST does not first seek a diskette drive, which saves about one second from the POST execution time.
- Disable Quiet Boot, which eliminates display of the logo splash screen. This could save several seconds of painting complex graphic images and changing video modes.
- Enabled Intel Rapid BIOS Boot. This feature bypasses memory count and the search for a diskette drive.

In the Peripheral Configuration submenu, disable the LAN device if it will not be used. This can reduce up to four seconds of option ROM boot time.

NOTE

It is possible to optimize the boot process to the point where the system boots so quickly that the Intel logo screen (or a custom logo splash screen) will not be seen. Monitors and hard disk drives with minimum initialization times can also contribute to a boot time that might be so fast that necessary logo screens and POST messages cannot be seen.

This boot time may be so fast that some drives might be not be initialized at all. If this condition should occur, it is possible to introduce a programmable delay ranging from three to 30 seconds (using the Hard Disk Pre-Delay feature of the Advanced Menu in the IDE Configuration Submenu of the BIOS Setup program).

3.9 BIOS Security Features

The BIOS includes security features that restrict access to the BIOS Setup program and who can boot the computer. A supervisor password and a user password can be set for the BIOS Setup program and for booting the computer, with the following restrictions:

- The supervisor password gives unrestricted access to view and change all the Setup options in the BIOS Setup program. This is the supervisor mode.
- The user password gives restricted access to view and change Setup options in the BIOS Setup program. This is the user mode.
- If only the supervisor password is set, pressing the <Enter> key at the password prompt of the BIOS Setup program allows the user restricted access to Setup.
- If both the supervisor and user passwords are set, users can enter either the supervisor password or the user password to access Setup. Users have access to Setup respective to which password is entered.
- Setting the user password restricts who can boot the computer. The password prompt will be displayed before the computer is booted. If only the supervisor password is set, the computer boots without asking for a password. If both passwords are set, the user can enter either password to boot the computer.

Table 47 shows the effects of setting the supervisor password and user password. This table is for reference only and is not displayed on the screen.

Table 47. Supervisor and User Password Functions

Password Set	Supervisor Mode	User Mode	Setup Options	Password to Enter Setup	Password During Boot
Neither	Can change all options (Note)	Can change all options (Note)	None	None	None
Supervisor only	Can change all options	Can change a limited number of options	Supervisor Password	Supervisor	None
User only	N/A	Can change all options	Enter Password Clear User Password	User	User
Supervisor and user set	Can change all options	Can change a limited number of options	Supervisor Password Enter Password	Supervisor or user	Supervisor or user

Note: If no password is set, any user can change all Setup options.

4 Error Messages and Beep Codes

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4.5 BIOS Beep Codes 82

4.1 BIOS Error Messages

Table 48 lists the error messages and provides a brief description of each.

Table 48. BIOS Error Messages

Error Message	Explanation
GA20 Error	An error occurred with Gate A20 when switching to protected mode during the memory test.
Pri Master HDD Error Pri Slave HDD Error Sec Master HDD Error Sec Slave HDD Error	Could not read sector from corresponding drive.
Pri Master Drive - ATAPI Incompatible Pri Slave Drive - ATAPI Incompatible Sec Master Drive - ATAPI Incompatible Sec Slave Drive - ATAPI Incompatible	Corresponding drive in not an ATAPI device. Run Setup to make sure device is selected correctly.
A: Drive Error	No response from diskette drive.
Cache Memory Bad	An error occurred when testing L2 cache. Cache memory may be bad.
CMOS Battery Low	The battery may be losing power. Replace the battery soon.
CMOS Display Type Wrong	The display type is different than what has been stored in CMOS. Check Setup to make sure type is correct.
CMOS Checksum Bad	The CMOS checksum is incorrect. CMOS memory may have been corrupted. Run Setup to reset values.
CMOS Settings Wrong	CMOS values are not the same as the last boot. These values have either been corrupted or the battery has failed.
CMOS Date/Time Not Set	The time and/or date values stored in CMOS are invalid. Run Setup to set correct values.
DMA Error	Error during read/write test of DMA controller.
FDC Failure	Error occurred trying to access diskette drive controller.
HDC Failure	Error occurred trying to access hard disk controller.

continued

Table 48. BIOS Error Messages (continued)

Error Message	Explanation
Checking NVRAM.....	NVRAM is being checked to see if it is valid.
Update OK!	NVRAM was invalid and has been updated.
Updated Failed	NVRAM was invalid but was unable to be updated.
Keyboard Error	Error in the keyboard connection. Make sure keyboard is connected properly.
KB/Interface Error	Keyboard interface test failed.
Memory Size Decreased	Memory size has decreased since the last boot. If no memory was removed then memory may be bad.
Memory Size Increased	Memory size has increased since the last boot. If no memory was added there may be a problem with the system.
Memory Size Changed	Memory size has changed since the last boot. If no memory was added or removed then memory may be bad.
No Boot Device Available	System did not find a device to boot.
Off Board Parity Error	A parity error occurred on an off-board card. This error is followed by an address.
On Board Parity Error	A parity error occurred in onboard memory. This error is followed by an address.
Parity Error	A parity error occurred in onboard memory at an unknown address.
NVRAM/CMOS/PASSWORD cleared by Jumper	NVRAM, CMOS, and passwords have been cleared. The system should be powered down and the jumper removed.
<CTRL_N> Pressed	CMOS is ignored and NVRAM is cleared. User must enter Setup.

4.2 Port 80h POST Codes

During the POST, the BIOS generates diagnostic progress codes (POST-codes) to I/O port 80h. If the POST fails, execution stops and the last POST code generated is left at port 80h. This code is useful for determining the point where an error occurred.

Displaying the POST-codes requires a PCI bus add-in card, often called a POST card. The POST card can decode the port and display the contents on a medium such as a seven-segment display.

NOTE

The POST card must be installed in PCI bus connector 1.

The tables below offer descriptions of the POST codes generated by the BIOS. Table 49 defines the uncompressed INIT code checkpoints, Table 50 describes the boot block recovery code checkpoints, and Table 51 lists the runtime code uncompressed in F000 shadow RAM. Some codes are repeated in the tables because that code applies to more than one operation.

Table 49. Uncompressed INIT Code Checkpoints

Code	Description of POST Operation
D0	NMI is Disabled. Onboard KBC, RTC enabled (if present). Init code Checksum verification starting.
D1	Keyboard controller BAT test, CPU ID saved, and going to 4 GB flat mode.
D3	Do necessary chipset initialization, start memory refresh, and do memory sizing.
D4	Verify base memory.
D5	Init code to be copied to segment 0 and control to be transferred to segment 0.
D6	Control is in segment 0. To check recovery mode and verify main BIOS checksum. If either it is recovery mode or main BIOS checksum is bad, go to check point E0 for recovery else go to check point D7 for giving control to main BIOS.
D7	Find Main BIOS module in ROM image.
D8	Uncompress the main BIOS module.
D9	Copy main BIOS image to F000 shadow RAM and give control to main BIOS in F000 shadow RAM.

Table 50. Boot Block Recovery Code Checkpoints

Code	Description of POST Operation
E0	Onboard Floppy Controller (if any) is initialized. Compressed recovery code is uncompressed in F000:0000 in Shadow RAM and give control to recovery code in F000 Shadow RAM. Initialize interrupt vector tables, initialize system timer, initialize DMA controller and interrupt controller.
E8	Initialize extra (Intel Recovery) Module.
E9	Initialize floppy drive.
EA	Try to boot from floppy. If reading of boot sector is successful, give control to boot sector code.
EB	Booting from floppy failed, look for ATAPI (LS-120, Zip) devices.
EC	Try to boot from ATAPI. If reading of boot sector is successful, give control to boot sector code.
EF	Booting from floppy and ATAPI device failed. Give two beeps. Retry the booting procedure again (go to check point E9).

Table 51. Runtime Code Uncompressed in F000 Shadow RAM

Code	Description of POST Operation
03	NMI is Disabled. To check soft reset/power-on.
05	BIOS stack set. Going to disable cache if any.
06	POST code to be uncompressed.
07	CPU init and CPU data area init to be done.
08	CMOS checksum calculation to be done next.
0B	Any initialization before keyboard BAT to be done next.
0C	KB controller I/B free. To issue the BAT command to keyboard controller.
0E	Any initialization after KB controller BAT to be done next.
0F	Keyboard command byte to be written.
10	Going to issue Pin-23,24 blocking/unblocking command.
11	Going to check pressing of <INS>, <END> key during power-on.
12	To init CMOS if "Init CMOS in every boot" is set or <END> key is pressed. Going to disable DMA and Interrupt controllers.
13	Video display is disabled and port-B is initialized. Chipset init about to begin.
14	8254 timer test about to start.
19	About to start memory refresh test.
1A	Memory Refresh line is toggling. Going to check 15 µs ON/OFF time.
23	To read 8042 input port and disable Megakey GreenPC feature. Make BIOS code segment writeable.
24	To do any setup before Int vector init.
25	Interrupt vector initialization to begin. To clear password if necessary.
27	Any initialization before setting video mode to be done.
28	Going for monochrome mode and color mode setting.
2A	Different buses init (system, static, output devices) to start if present. (See Section 4.3 for details of different buses.)
2B	To give control for any setup required before optional video ROM check.
2C	To look for optional video ROM and give control.
2D	To give control to do any processing after video ROM returns control.
2E	If EGA/VGA not found then do display memory R/W test.
2F	EGA/VGA not found. Display memory R/W test about to begin.
30	Display memory R/W test passed. About to look for the retrace checking.
31	Display memory R/W test or retrace checking failed. To do alternate Display memory R/W test.
32	Alternate Display memory R/W test passed. To look for the alternate display retrace checking.
34	Video display checking over. Display mode to be set next.
37	Display mode set. Going to display the power-on message.
38	Different buses init (input, IPL, general devices) to start if present. (See Section 4.3 for details of different buses.)
39	Display different buses initialization error messages. (See Section 4.3 for details of different buses.)
3A	New cursor position read and saved. To display the Hit <DEL> message.

continued

Table 51. Runtime Code Uncompressed in F000 Shadow RAM (continued)

Code	Description of POST Operation
40	To prepare the descriptor tables.
42	To enter in virtual mode for memory test.
43	To enable interrupts for diagnostics mode.
44	To initialize data to check memory wrap around at 0:0.
45	Data initialized. Going to check for memory wrap around at 0:0 and finding the total system memory size.
46	Memory wrap around test done. Memory size calculation over. About to go for writing patterns to test memory.
47	Pattern to be tested written in extended memory. Going to write patterns in base 640k memory.
48	Patterns written in base memory. Going to find out amount of memory below 1M memory.
49	Amount of memory below 1M found and verified. Going to find out amount of memory above 1M memory.
4B	Amount of memory above 1M found and verified. Check for soft reset and going to clear memory below 1M for soft reset. (If power on, go to check point # 4Eh).
4C	Memory below 1M cleared. (SOFT RESET) Going to clear memory above 1M.
4D	Memory above 1M cleared. (SOFT RESET) Going to save the memory size. (Go to check point # 52h).
4E	Memory test started. (NOT SOFT RESET) About to display the first 64k memory size.
4F	Memory size display started. This will be updated during memory test. Going for sequential and random memory test.
50	Memory testing/initialization below 1M complete. Going to adjust displayed memory size for relocation/shadow.
51	Memory size display adjusted due to relocation/ shadow. Memory test above 1M to follow.
52	Memory testing/initialization above 1M complete. Going to save memory size information.
53	Memory size information is saved. CPU registers are saved. Going to enter in real mode.
54	Shutdown successful, CPU in real mode. Going to disable gate A20 line and disable parity/NMI.
57	A20 address line, parity/NMI disable successful. Going to adjust memory size depending on relocation/shadow.
58	Memory size adjusted for relocation/shadow. Going to clear Hit <DEL> message.
59	Hit <DEL> message cleared. <WAIT...> message displayed. About to start DMA and interrupt controller test.
60	DMA page register test passed. To do DMA#1 base register test.
62	DMA#1 base register test passed. To do DMA#2 base register test.
65	DMA#2 base register test passed. To program DMA unit 1 and 2.
66	DMA unit 1 and 2 programming over. To initialize 8259 interrupt controller.
7F	Extended NMI sources enabling is in progress.
80	Keyboard test started. Clearing output buffer, checking for stuck key, to issue keyboard reset command.
81	Keyboard reset error/stuck key found. To issue keyboard controller interface test command.
82	Keyboard controller interface test over. To write command byte and init circular buffer.
83	Command byte written, global data init done. To check for lock-key.

continued

Table 51. Runtime Code Uncompressed in F000 Shadow RAM (continued)

Code	Description of POST Operation
84	Lock-key checking over. To check for memory size mismatch with CMOS.
85	Memory size check done. To display soft error and check for password or bypass setup.
86	Password checked. About to do programming before setup.
87	Programming before setup complete. To uncompress SETUP code and execute CMOS setup.
88	Returned from CMOS setup program and screen is cleared. About to do programming after setup.
89	Programming after setup complete. Going to display power-on screen message.
8B	First screen message displayed. <WAIT...> message displayed. PS/2 Mouse check and extended BIOS data area allocation to be done.
8C	Setup options programming after CMOS setup about to start.
8D	Going for hard disk controller reset.
8F	Hard disk controller reset done. Floppy setup to be done next.
91	Floppy setup complete. Hard disk setup to be done next.
95	Init of different buses optional ROMs from C800 to start. (See Section 4.3 for details of different buses.)
96	Going to do any init before C800 optional ROM control.
97	Any init before C800 optional ROM control is over. Optional ROM check and control will be done next.
98	Optional ROM control is done. About to give control to do any required processing after optional ROM returns control and enable external cache.
99	Any initialization required after optional ROM test over. Going to setup timer data area and printer base address.
9A	Return after setting timer and printer base address. Going to set the RS-232 base address.
9B	Returned after RS-232 base address. Going to do any initialization before Coprocessor test.
9C	Required initialization before Coprocessor is over. Going to initialize the Coprocessor next.
9D	Coprocessor initialized. Going to do any initialization after Coprocessor test.
9E	Initialization after Coprocessor test is complete. Going to check extended keyboard, keyboard ID and num-lock.
A2	Going to display any soft errors.
A3	Soft error display complete. Going to set keyboard typematic rate.
A4	Keyboard typematic rate set. To program memory wait states.
A5	Going to enable parity/NMI.
A7	NMI and parity enabled. Going to do any initialization required before giving control to optional ROM at E000.
A8	Initialization before E000 ROM control over. E000 ROM to get control next.
A9	Returned from E000 ROM control. Going to do any initialization required after E000 optional ROM control.
AA	Initialization after E000 optional ROM control is over. Going to display the system configuration.
AB	Put INT13 module runtime image to shadow.
AC	Generate MP for multiprocessor support (if present).
AD	Put CGA INT10 module (if present) in Shadow.

continued

Table 51. Runtime Code Uncompressed in F000 Shadow RAM (continued)

Code	Description of POST Operation
AE	Uncompress SMBIOS module and init SMBIOS code and form the runtime SMBIOS image in shadow.
B1	Going to copy any code to specific area.
00	Copying of code to specific area done. Going to give control to INT-19 boot loader.

4.3 Bus Initialization Checkpoints

The system BIOS gives control to the different buses at several checkpoints to do various tasks. Table 52 describes the bus initialization checkpoints.

Table 52. Bus Initialization Checkpoints

Checkpoint	Description
2A	Different buses init (system, static, and output devices) to start if present.
38	Different buses init (input, IPL, and general devices) to start if present.
39	Display different buses initialization error messages.
95	Init of different buses optional ROMs from C800 to start.

While control is inside the different bus routines, additional checkpoints are output to port 80h as WORD to identify the routines under execution. In these WORD checkpoints, the low byte of the checkpoint is the system BIOS checkpoint from which the control is passed to the different bus routines. The high byte of the checkpoint is the indication of which routine is being executed in the different buses. Table 53 describes the upper nibble of the high byte and indicates the function that is being executed.

Table 53. Upper Nibble High Byte Functions

Value	Description
0	func#0, disable all devices on the bus concerned.
1	func#1, static devices init on the bus concerned.
2	func#2, output device init on the bus concerned.
3	func#3, input device init on the bus concerned.
4	func#4, IPL device init on the bus concerned.
5	func#5, general device init on the bus concerned.
6	func#6, error reporting for the bus concerned.
7	func#7, add-on ROM init for all buses.

Table 54 describes the lower nibble of the high byte and indicates the bus on which the routines are being executed.

Table 54. Lower Nibble High Byte Functions

Value	Description
0	Generic DIM (Device Initialization Manager)
1	On-board System devices
2	ISA devices
3	EISA devices
4	ISA PnP devices
5	PCI devices

4.4 Speaker

A 47 Ω inductive speaker provides audible error code (beep code) information during POST.

For information about	Refer to
The location of the onboard speaker on the Desktop Board D845GVFN	Figure 1, on page 12

4.5 BIOS Beep Codes

Whenever a recoverable error occurs during POST, the BIOS displays an error message describing the problem (see Table 55). The BIOS also issues a beep code (one long tone followed by two short tones) during POST if the video configuration fails (a faulty video card or no card installed) or if an external ROM module does not properly checksum to zero.

An external ROM module (for example, a video BIOS) can also issue audible errors, usually consisting of one long tone followed by a series of short tones. For more information on the beep codes issued, check the documentation for that external device.

There are several POST routines that issue a POST terminal error and shut down the system if they fail. Before shutting down the system, the terminal-error handler issues a beep code signifying the test point error, writes the error to I/O port 80h, attempts to initialize the video and writes the error in the upper left corner of the screen (using both monochrome and color adapters).

If POST completes normally, the BIOS issues one short beep before passing control to the operating system.

Table 55. Beep Codes

Beep	Description
1	Refresh failure
2	Parity cannot be reset
3	First 64 KB memory failure
4	Timer not operational
5	Not used
6	8042 GateA20 cannot be toggled
7	Exception interrupt error
8	Display memory R/W error
9	Not used
10	CMOS Shutdown register test error
11	Invalid BIOS (e.g. POST module not found, etc.)